operation. The if output of transistor Q24 is sent to AGC/AM audio detector, transistor Q25. Also, the if signal at the emitter of Q24 is coupled to transistor Q28 of the SSB detector, which is comprised of transistors Q26, Q27, and Q28. The SSB detector is switched on during USB mode by RCV·$\overline{AM}$ logic (P2-12) which is applied to the base of transistor Q27. The 5-MHz injection signal from P1-21 is coupled to the base of Q26. Mixing the injection frequency with the receive if produces the resultant USB af output from Q27 which is then coupled by capacitor C54 to switch U3C. During USB receive mode, switch U3C is closed by RCV·$\overline{AM}$ logic and the audio output of U3C is coupled to the audio amplifiers by capacitor C55. The USB audio amplifiers are the same ones that are used for AM operation.

1.7.4.2.2 Transmitter Theory

The receiver-transmitter group is ready to transmit after power is turned on, frequency and mode are selected at control A2, and tuning is complete. To transmit, enable the receiver-transmitter group keyline by (1) pressing the ptt switch on the headset or handset, or (2) by keying the telegraph key.

Refer to figures 4-1, 4-6, and 4-14 schematic section. For voice operation, the PTT signal is supplied to A1A5A2 from control A2 through the following route; A2P1/A1A1J1-39, through chassis A1A1 wiring to A1A1J5/A1A5A1P1-23, and through A1A5A1 board wiring to A1A5A1P2/A1A5A2P1-26.

For CW keying operation, the CW KEY signal is supplied to A1A5A2 from control A2 through the following route; A2P1/A1A1J1-19, through A1A1 chassis wiring to A1A1J5/A1A5A1P1-17 and through A1A5A1 board wiring to A1A5A1P2/A1A5A2P1-20.

For xmit audio (voice), the xmit audio signal is supplied to A1A5A2 from control A2 through the following route; A2P1/A1A1J1-20, through chassis A1A1 wiring to A1A1J5/A1A5A1P1-15, and through A1A5A1 board wiring to A1A5A1P2/A1A5A2P1-29.

1.7.4.2.2.1 Logic/Tx A1A5A2

Refer to figure 1-12 of this section and figure 4-6, schematics section. XMT AUDIO from P1-29 is coupled through FET Q12 to af amplifier U8B. Transistor Q14 and FET Q13 serve as a voice/data gain change stage (data is not used). The af output from amplifier U8B is applied to P1-9 and to af amplifier U8A. The audio to U8A is amplified and applied to AGC detector, transistor Q11. The AGC detector output voltage is applied to attenuators (FET's Q12 and Q15) to maintain the audio output at P1-9 at a constant level.

Figure 1-10 of this section provides a logic table for the various transmit-receive functions. In CW mode, the 2-kHz audio from P1-10 passes through gate/filter stage, FET's Q5, Q6, and Q16, and through af amplifier U8B with attenuators Q12 and Q15 at full attenuation. RC network C1 and R4 provides a delay to hold the radio in transmit mode for approximately one second after CW key is released.

The rechannel pulse signal at P1-24, which is momentary ground, causes capacitors C4 and C24 to be discharged by transistors Q3 and Q4, respectively. The output pulse at P1-33 ($\overline{RCP\ STRETCH}$) is delayed by the time constand of C4 and R18 and the pulse width is determined by C24 and R69.

1.7.4.2.2.2 If/Af A1A5A1

Refer to figure 1-10 and 1-11 in this section. The logic in transmit turns on balanced modulator U1 and transistor Q3, while biasing off transistor Q39. The XMT AUDIO from P2-9 is applied to balanced modulator U1 where it is mixed with 5-MHz from P1-21 to produce a double sideband, suppressed carrier output signal. This output signal from U1 is sent through transistor Q5, diode CR2 and SSB filter FL2.

PI PIN	INPUTS						OUTPUTS	
	PTT 26	TIP 28	CW KEY 20	RCV ONLY 15	XMT INH 22	TUNE FAULT 17	RCV 6	XMT 32
	X	X	X	X	X	0	X	0
	0	X	X	X	X	0	0	X
	X	0	X	X	X	0	0	X
	0	X	X	0	X	0	X	0
	0	X	X	X	0	0	X	0
	0	X	X	X	X	X	X	0
	X	X	0	X	X	0	0	X
	X	X	0 TO X	X	X	0	NOTE	NOTE

NOTE: WHEN CW KEY IS DISABLED THE OUTPUT STAYS AT ZERO AT PI-6 FOR APPROX. 1 SECOND.

X = MORE THAN +4.5 V
0 = LESS THAN +0.5 V

PI PIN	INPUTS			OUTPUTS				
	PTT 26	AM 19	TIP 28	13	30	27	12	23
	X	X	X	0	X	0	X	0
	0	X	X	0	X	0	0	X
	X	0	X	X	0	0	0	X
	0	0	X	0	X	X	0	X
	X	0	0	X	0	0	0	X

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Figure 1-10. Logic/Tx A1A5A2, Logic Tables

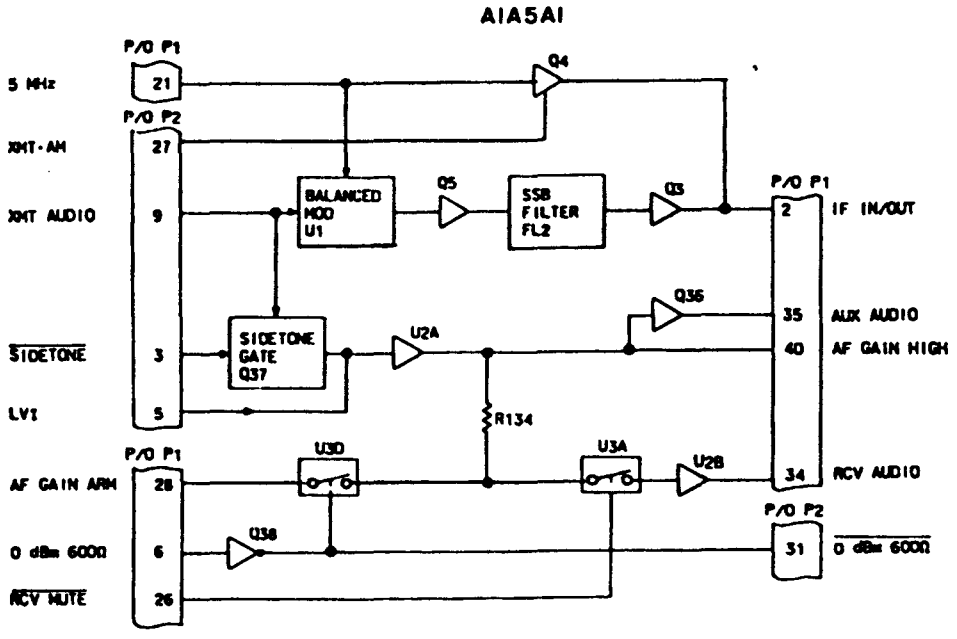


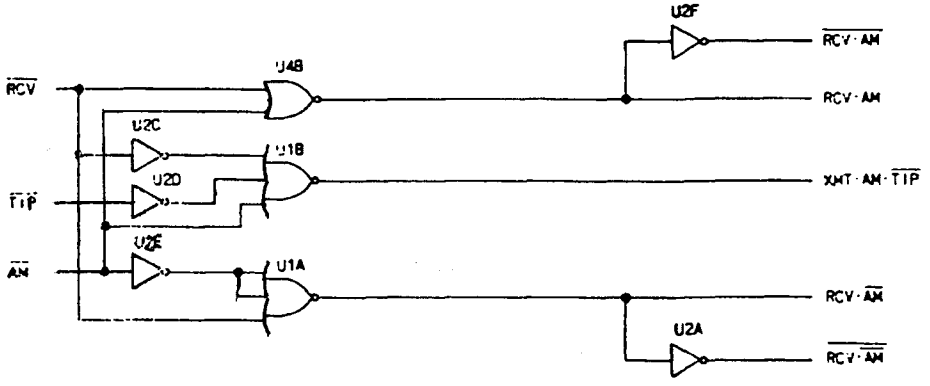
Figure 1-11. If/Af A1A5A1 (Transmit), Simplified Schematic Diagram

The if output from FL2 is amplified by transistor Q3 and coupled to P1-2 (IF OUT). If AM is selected at control A2, carrier reinsert gate, transistor Q4 and diode CR1, are gated on by logic from P2-27. This allows the 5-MHz carrier to be added to the SSB output of if amplifier Q3, producing an AM equivalent (AM) signal to P1-2.

a. Sidetone and Low Voltage Input. During transmit, the sidetone transmit audio is supplied to the headset or the handset via the receive audio circuits previously discussed. Refer to figures 1-12 and 1-13 of this section and figures 4-5 and 4-6, schematics section.

There are three conditions when the sidetone gate (FET A1A5A1Q37) is biased on: When (1) tuning is in progress (TIP) a 2-kHz tone is heard; when (2) a coupler fault occurs, a pulsating 2-kHz tone is heard; or, when (3) there is forward power output from amplifier-coupler (A3), audio is heard. In USB mode FET A1A5A1Q37 remains on for the time constant of capacitor A1A5A2C3 and resistor A1A5A2R14 (approximately 1 second) after the absence of voice audio.

The low voltage input (LVI) indication occurs when +25.2 V dc (SW) at A1A5A2P1-25 becomes less than +22.5 volts, allowing transistor A1A5A2Q1 to conduct. This causes square-wave generator A1A5A2U4A and A1A5A2U5A to oscillate. This square-wave output is coupled through R37 to A1A5A2P1/A1A5A1P2-5 and on to the audio circuits of A1A5A1 to produce a low frequency clicking sound. If a coupler fault occurs during this time, a pulsating 2-kHz tone is heard.



INPUTS		
AM	TIP	RCV
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS				
RCV·AM	RCV·AM	XMT·AM·TIP	RCV·AM	RCV·AM
0	1	0	1	0
1	0	0	1	0
0	1	0	1	0
1	0	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	0	0	1
1	0	0	1	0

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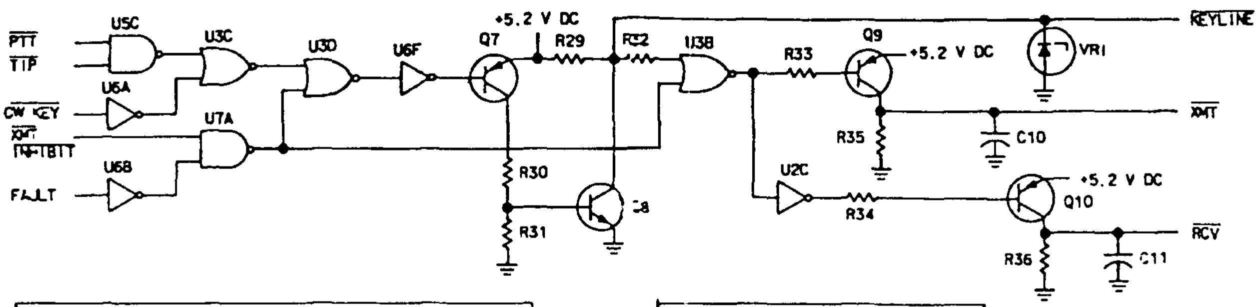
Figure 1-12. Logic/Tx A1A5A2, Simplified Schematic Diagram and Logic Tables



INPUTS				
PTT	TIP	CW KEY	XMT INHIBIT	FAULT
0	0	0	0	0
0	0	0	0	1
0	0	0	1	0
0	0	0	1	1
0	0	1	0	0
0	0	1	0	1
0	0	1	1	0
0	0	1	1	1
0	1	0	0	0
0	1	0	0	1
0	1	0	1	0
0	1	0	1	1
0	1	1	0	0
0	1	1	0	1
0	1	1	1	0
0	1	1	1	1
1	0	0	0	0
1	0	0	0	1
1	0	0	1	0
1	0	0	1	1
1	0	1	0	0
1	0	1	0	1
1	0	1	1	0
1	0	1	1	1
1	1	0	0	0
1	1	0	0	1
1	1	0	1	0
1	1	0	1	1
1	1	1	0	0
1	1	1	0	1
1	1	1	1	0
1	1	1	1	1

OUTPUTS		
KEYLINE	XMT	RCV
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
1	1	0
1	1	0

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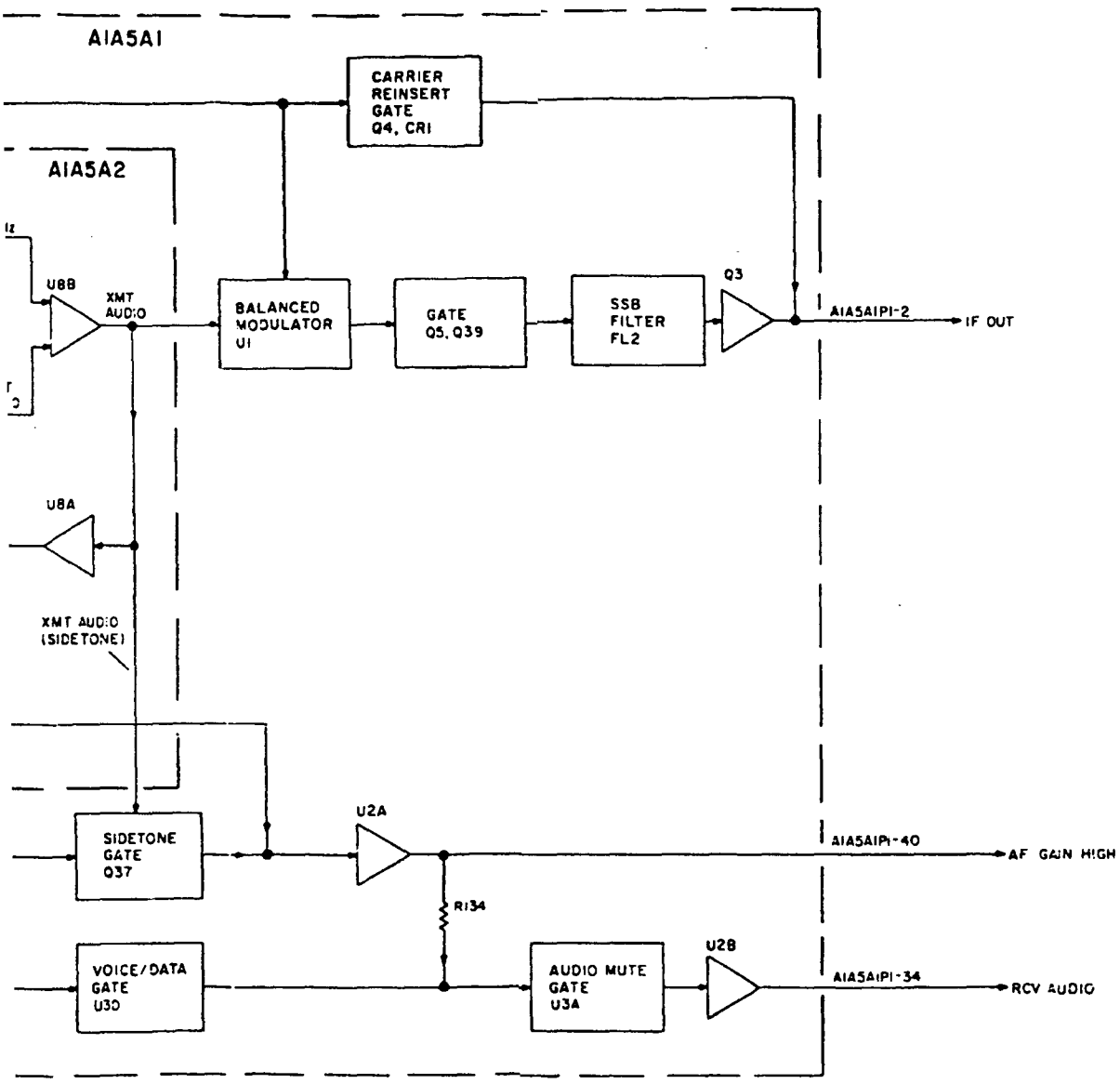

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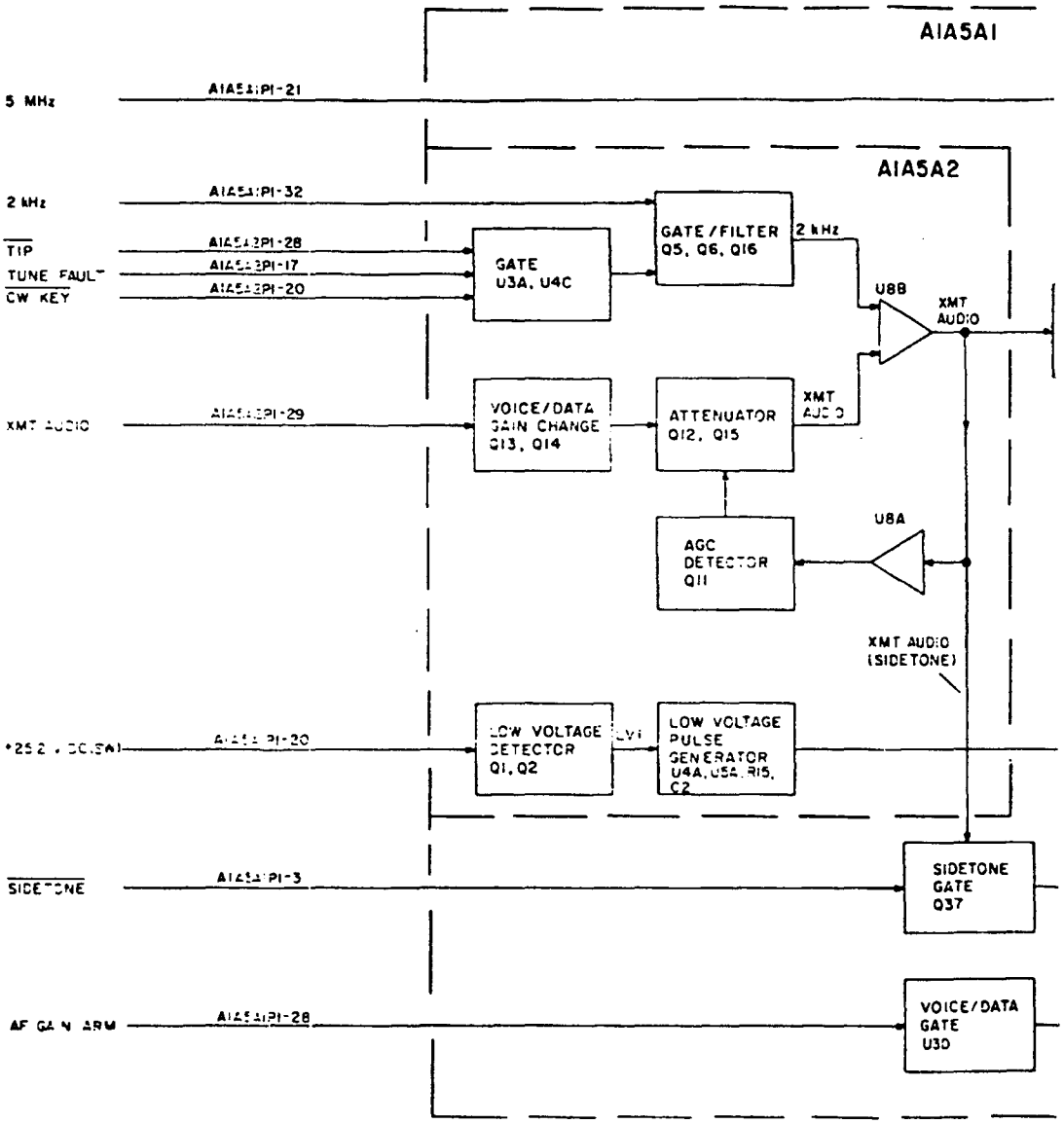
Figure 1-13. If/Af Amplifier A1A5 (Transmit) Functional Block Diagram


A1A5A1
5 MHz
A1A5A1P1-21
A1A5A2
2 kHz
A1A5A1P1-32
TIP
TUNE FAULT
CW KEY
A1A5A2P1-28
A1A5A2P1-17
A1A5A2P1-20
GATE
U3A, U4C
GATE/FILTER
Q5, Q6, Q16
2 kHz
U8B
XMT
AUDIO
XMT AUDIO
A1A5A2P1-29
VOICE/DATA
GAIN CHANGE
Q13, Q14
ATTENUATOR
Q12, Q15
XMT
AUDIO
U8A
AGC
DETECTOR
Q11
XMT AUDIO
(SIDETONE)
+25.2 ± 20.5VDC
A1A5A1P1-20
LOW VOLTAGE
DETECTOR
Q1, Q2
LVI
LOW VOLTAGE
PULSE
GENERATOR
U4A, U5A, R15,
C2
SIDETONE
A1A5A1P1-3
SIDETONE
GATE
Q37
AF GAIN ARM
A1A5A1P1-28
VOICE/DATA
GATE
U3D

b. ALC. Refer to figure 1-14 of this section and figure 4-5 of the schematic section. During transmit operation, the ALC stages of A1A5A1 are enabled by XMT logic from P2-32 to switch transistor Q11. When transmitting, negative ALC voltage from amplifier-coupler A3 is applied from P1-31 to the emitter of transistor Q17. If broadband amplifier A1A3 exceeds approximately 300 mW, it develops a negative ALC voltage which is applied to the emitter of transistor Q16 through P1-36. The output of Q16 or Q17 causes transistor Q13 to start discharging capacitor C22, which causes transistor Q9 to begin conduction. As the conduction of Q9 increases, the output of transistor Q6 (ALC/AGC DRIVE to mixer A1A2) decreases, permitting diodes A1A2CR1 and A1A2CR7 to conduct. This decreases the rf output from A1A2 to amplifier-coupler A3 until A3 has the proper output level and is not overdriven.

1.7.4.2.2.3 Mixer A1A2

Refer to figure 1-8 of this section and figure 4-2 of the schematic section. During transmit, the switching logic at P1-5 and P1-6 switches the transmit mixers on and the receive mixers off. The IF IN (5-MHz AME or SSB) signal is coupled by diode CR10 and transformer T8 to the up conversion mixer, transistors Q15 and Q16. The sum of 110- and 5-MHz frequencies (115 MHz) is coupled through transformer T7 and diode CR9 to the 115-MHz filter. The filtered output is coupled to the down conversion mixer, FET's Q5 and Q8, by diode CR5 and transformer T4. Here the 115-MHz signal is mixed with 117- to 144.9999-MHz variable injection signal from P2 to obtain the 2- to 29.9999-MHz output. FET's Q7 and Q8 neutralize

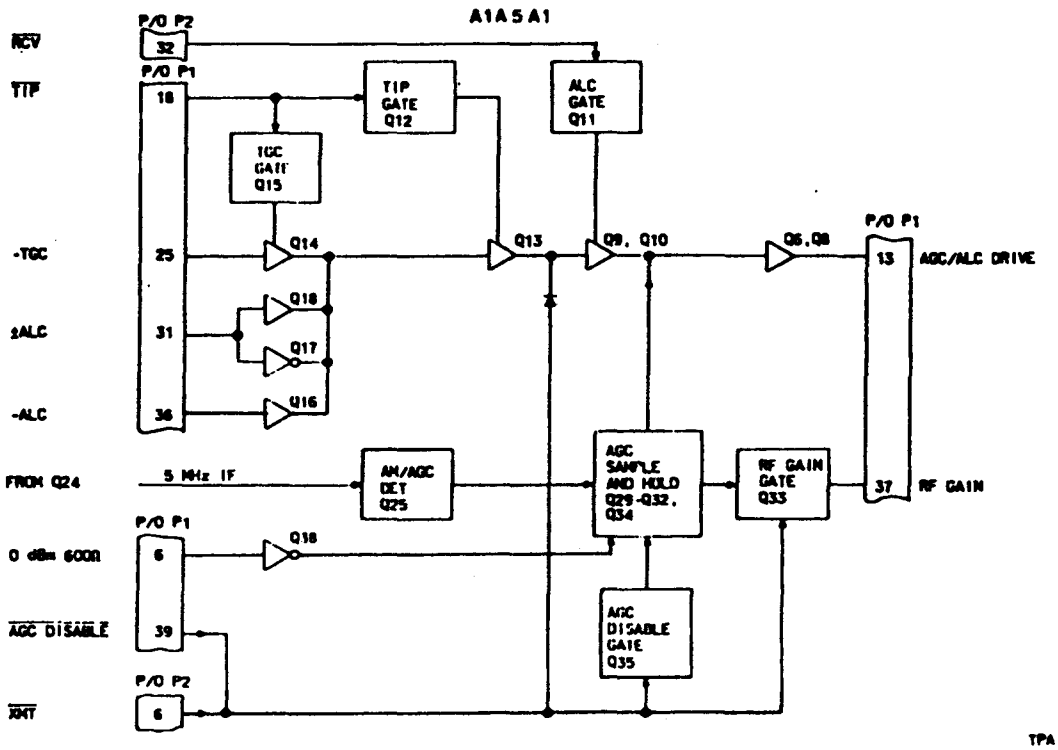


Figure 1-14. AGC/ALC, Simplified Schematic Diagram

the gate-to-drain capacity of FET's Q5 and Q6. The rf output of the down conversion mixer is coupled through low-pass filter inductors L1 and L2 and capacitors C1 and C2, to P1-14 (XMT RF) by transformer T3, diode CR4, and capacitor C4. If the rf output is too high (as noted in ALC discussion), the ALC/ AGC DRIVE at P1-9 decreases, permitting diodes CR1 and CR7 to conduct, reducing the rf output.

1.7.4.2.2.4 Broadband Amplifier A1A3

Refer to figure 1-7 of this section and figures 4-1 and 4-3 of the schematic section. The transmit rf output of A1A2 is applied to A1A3 via A1A2P1/A1A1J2-14 and A1A1J3/A1A3P1-2. With the radio turned on at the control, +25.2 V dc (SW) is applied to A1A3, and with the key line enabled by the ptt switch, keying relay K1 is energized and the +25.2 V dc (SW) is switched to the amplifier circuits by Q4. The incoming rf at P1-2 is passed through the LC filter network, a limiter circuit and on to the emitter follower stage, Q1, through the closed relay contacts, B1 and B2. The emitter follower couples the rf to rf amplifiers Q2, Q3, and Q5. The 250-mW rf output of Q5 is transformer coupled by T1 through the closed relay contacts A1 and A2 to P1-12. The ALC detector, VR2 and CR8, provide a protective ALC bias to A1A5 ALC circuits that limits the rf output to approximately 300 mW if amplifier-coupler A3 ALC should fail. This ALC OUT signal at P1-9 is routed through A1A1J3-9 to A1A1J5/A1A5A1P1-36. The transmit rf output from A1A3 is supplied to amplifier-coupler A3 through A1A3P1/A1A1J3-12 of A1A3 and A1A1P1/A3J1-36.

1.7.4.2.2.5 Frequency Synthesizer A1A6

Refer to figure 1-6. Frequency synthesizer A1A6 provides a variable injection frequency and a fixed injection frequency to A1A2 plus two fixed frequencies to A1A5 during both receive and transmit periods of operation. The variable injection frequency is a frequency in the 117 MHz to 144.9999-MHz range, variable in 100-Hz increments, the specific frequency being proportionate to the operating frequency selected at the control. The fixed injection frequency to the mixer module is 110 MHz. Two fixed frequencies are supplied to A1A5. One is the 5-MHz fixed injection frequency and the other one is the 2-kHz tone signal. A1A6 also supplies the transmit inhibit logic output (XMT INH) in response to the power on or frequency change logic (RECHANNEL) from control A2. Control A2 also provides the bcd frequency selection logic and the USB logic inputs to A1A6.

To process the above logic inputs and to generate the above output signals, the frequency synthesizer uses the seven subassemblies shown on figure 1-6. For frequency generation functions, four phase-lock loops are used. Refer to figure 1-15. One phase-lock loop is used to generate the fixed injection frequency (110 MHz). The remaining phase-lock loops, the low frequency, the converter, and the high frequency phase-lock loops, are used to generate the 117-144.9999-MHz variable injection frequency. The low frequency phase-lock loop (LFPLL) uses the bcd logic from the control and provides the bcd selected frequency within the 1.0 to 1.0999-MHz range to the converter for translation to a higher frequency within the 111 to 111.0999-MHz range.

This translated output from the converter is applied to the high frequency phase-lock loop (HFPLL) for translation to a higher frequency. During locked conditions, the HFPLL is controlled by the sample and hold phase detector stage. The output frequency of the HFPLL mixer (variable from 6-33.9 MHz), the resultant frequency of mixing the output frequency of the converter (111-111.0999 MHz) with the HFPLL vco frequency (117-144.9999 MHz), is sampled by the sample and hold phase detector to maintain the correct vco frequency. But, when a new frequency acquisition by the HFPLL is required (initiated by frequency change at control A2), control of the HFPLL vco is switched to the frequency/phase discriminator of the variable divider to acquire digital phase lock on the new frequency. As shown in figure 1-15, the variable divider is controlled by bcd logic from the control, thus, a frequency

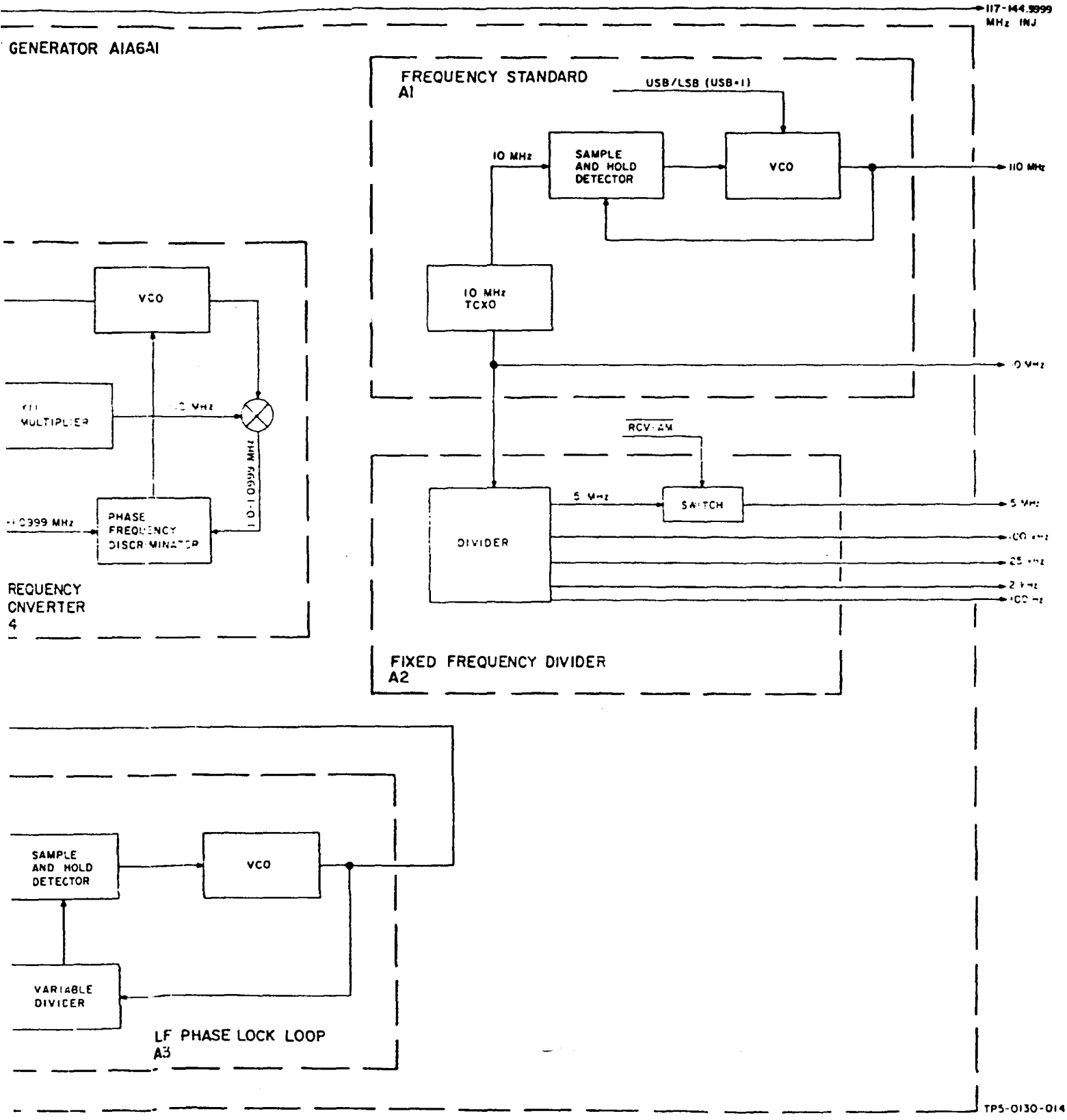
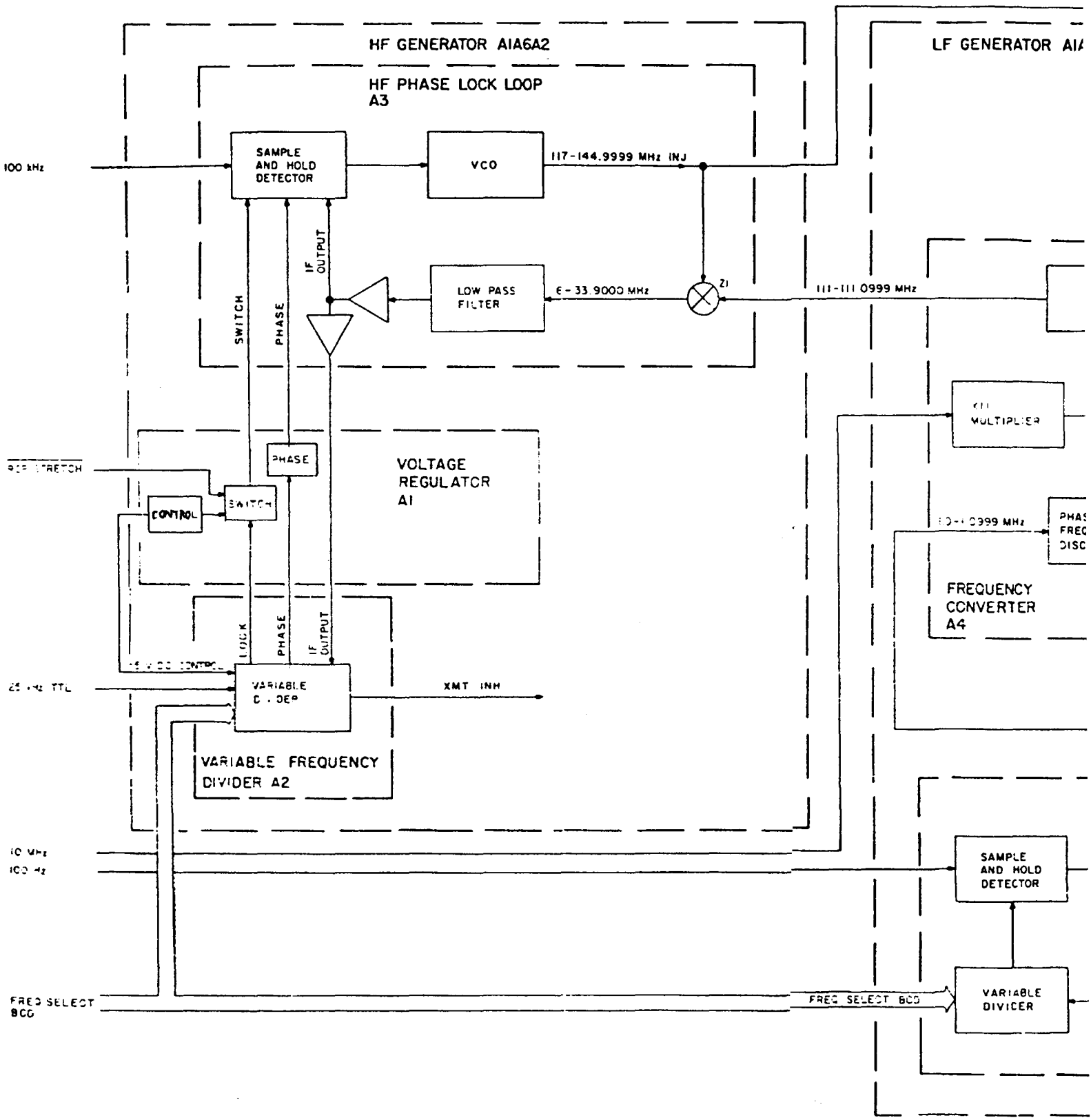


Figure 1-15. Frequency Synthesizer A1A6, Block Diagram


HF GENERATOR AIA6A2
HF PHASE LOCK LOOP
A3
LF GENERATOR AIA
100 kHz
SAMPLE
AND HOLD
DETECTOR
VCO
117-144.9999 MHz INJ
IF
OUTPUT
SWITCH
PHASE
LOW PASS
FILTER
6-33.9000 MHz
ZI
111-111.0999 MHz
MULTIPLIER
PHASE
VOLTAGE
REGULATOR
A1
CONTROL
SWITCH
LOCK
PHASE
IF
OUTPUT
FREQUENCY
CONVERTER
A4
VARIABLE
DIVIDER
XMT INH
VARIABLE FREQUENCY
DIVIDER A2
SAMPLE
AND HOLD
DETECTOR
VARIABLE
DIVIDER
FREQ SELECT
BCD
FREQ SELECT BCD

change at the control causes the bcd logic change to switch on the variable divider. This initiates the loop action necessary to achieve digital phase lock on the new frequency by the frequency/phase discriminator and inhibit the transmit (XMT INH) functions during frequency acquisition (rechannel cycle). When digital phase-lock occurs, vco control is transferred back to the sample and hold phase detector and the variable divider is switched off. This puts the hf phase-lock loop back in a locked (normal) condition.

The fixed divider operates in conjunction with the frequency standard and supplies the following frequencies to the radio receiver-transmitter. The 5-MHz is supplied to A1A5 during all modes of operation except AM receive when the 5-MHz signal is switched off. The 2-kHz tone signal is supplied to A1A5 during all modes of operation. The 100-kHz frequency is supplied to the HFPLL. The 25-kHz frequency is applied to the variable divider, and the 100-Hz frequency is supplied to the LFPLL.

a. Frequency Standard A1A6A1A1. Refer to figures 1-6 and 1-15 of this section, and figure 4-7, schematics section. The frequency standard subassembly circuits are comprised of the frequency standard generator (10 MHz), which is a temperature-compensated, crystal controlled oscillator (texo), and a fixed injection frequency generator, which is a vco with a sample and hold stage. The texo consists of crystal Y1, transistors Q1 and Q2, varactor CR2 and temperature compensating networks RT1, RT2, and RT3. The trimmer capacitor is provided to compensate for the aging of the crystal and the selectable components (as noted by schematic note 3) are to be selected at final test. When the radio power is turned on, the texo is energized and supplies a stable reference frequency of 10 MHz from the impedance matching output network of Q1 and Q2 through the buffer-driver stage Q3 and Q4 to the sample and hold reference pulse shaper Q5. The 10-MHz reference frequency output from the impedance matching network is supplied to frequency converter A1A6A1A4 and the 10-MHz output from the buffer-driver is applied to A1A6A1A2. The vco circuit consists of the oscillator, FET Q9, varactor CR1, and switch transistor Q8. With the radio power on, the USB logic input from A1A5 switches transistor Q8 on to provide the correct dc voltage level for the oscillator to operate at 110 MHz. The 110-MHz output of the vco is applied to the sample and hold circuit, CR7 and CR8, through buffer Q6 and Q7. The rectifier diodes CR7 and CR8, provide a negative dc voltage feedback to the vco that corrects the frequency compared to the 10-MHz reference frequency at the primary of T1. The 110-MHz output from the vco, 110 MHz INJ, is applied to A1A2 as an output from buffer-driver Q10 and connector A1A6A1A1P1.

The +5.2 V dc is supplied to frequency standard A1A6A1A1 from power supply A1A4 via A1A1 and A1A6A1A2. The +11.5 V dc is supplied by voltage regulator A1A6A2A1 via A1A6A1A2. (Refer to figure 4-11, schematics section.)

b. Fixed Frequency Divider A1A6A1A2. Refer to figures 1-6 and 1-15 of this section and figure 4-8, schematics section. The fixed frequency divider consists of a network of frequency dividers and a gated transistor emitter-follower circuit that applies the 5-MHz injection frequency output to A1A5. The 10-MHz reference frequency is supplied by A1A6A1A1 to transistor driver Q2. The output of the driver is a 10-MHz square-wave clocking signal that is applied to the 2:1 frequency divider, U1A. The outputs of the divider are two 5-MHz signals. One is used to clock the 5:1 divider stage, U1B and U2, and the other is coupled to emitter-follower Q1, which is controlled by the $\overline{\text{RCV}\cdot\text{AM}}$ logic from P1-6. Q1 is turned on by the $\overline{\text{RCV}\cdot\text{AM}}$ logic during all modes of operation except the AM receive mode at which time Q1 is turned off and the 5-MHz output is cut off. The 5-MHz input to the dividers, U1B, U2A and U2B, is divided by 5, to 1 MHz, and further divided by 10, to 100-kHz, by U3A. One 100-kHz output is applied to divider U3B and one output is supplied to HFPLL A1A6A2A3. The divider U3B is configured to divide the 100-kHz signal by 2 and 5, providing a 50-kHz output and a 20-kHz

output. The 50-kHz output is divided by 2 by U4A to provide a 25-kHz frequency to the variable divider subassembly. The 20-kHz output is applied to divider U5B and divided by 10 to produce a 2-kHz output. This is coupled by capacitor C2 to P1-5.

The 2-kHz output from divider U5B is also applied to 2:1 divider U4B and to 10:1 divider U5A, and converted to 100 Hz for application to LFPLL A1A6A1A3.

The +5.2 V dc is supplied by A1A4 and the +11.5 V dc is provided by A1A6A2A1 (figure 4-11, schematics section).

c. LF Phase-Lock Loop A1A6A1A3. Refer to figures 1-6 and 1-15 of this section and figure 4-9, schematics section. The LFPLL supplies to the frequency converter A1A6A1A4 a frequency that can be varied from 1.0 MHz to 1.0999 MHz in 100-Hz increments. The specific frequency within the 1.0- to 1.0999-MHz range is determined by the bcd logic input to connector P1 from control A2. To generate the 1.0- to 1.09999 MHz frequency, A1A6A1A3 employs a vco stage, a frequency/phase detector stage, and a sample and hold phase detector stage referenced to 100-Hz from the fixed frequency divider. The output frequency of the vco is controlled over the above range by the dc voltage applied to varactor CR2. Therefore, when a frequency is selected at control A2, the bcd logic is applied to the frequency discriminator variable dividers U6-U9. They establish the proper logic input to the sample and hold switch, U1, to adjust the dc voltage to CR2 for an oscillator output frequency equivalent to the binary coding from control A2. To maintain vco frequency stability, the output of the vco is looped back to the phase detector, U4A, through feedback driver Q7. The output of the frequency discriminator is applied from NOR gate U5A to the phase detector U4A. The output of U4A is a logic output with a variable duty cycle that controls the duty cycle of the output from U6 to the sample and hold phase detector, U1. Also applied to U1 is the ramp voltage supplied by the ramp generator, transistors Q1 and Q2. The ramp generator is driven by the 100-Hz reference signal from A1A6A1A2. When Q2 is on (the input is high), capacitors C1 and C2 are held at zero. When the input is low Q1 is turned off, allowing C1 and C2 to charge toward 14 V dc at a constant rate until Q2 is turned on by the 100-Hz input. The ramp voltage is sampled by the ϕ1 and ϕ2 signals at the duty cycle rate which is a function of the phase difference between the compared frequencies applied to the phase detector, U4A. The ϕ1 signal gates (samples) the ramp voltage through the first part of switch U1. The ϕ2 signal follows and gates the sampled ramp voltage through the second section of switch U1 for filtering. The sampled ramp voltage, after filtering, becomes the vco control voltage and is coupled to varactor CR2 by source followers Q3 and Q4. Increasing the vco control voltage, increases the vco frequency; decreasing the control voltage, decreases the vco frequency. Therefore, the vco control voltage, being a function of the frequency difference between the compared frequencies, increases or decreases the oscillator frequency to correct the output frequency.

The +13 V dc voltage is supplied by A1A4 and the +11.5 and +14 V dc voltage is provided by A1A6A2A1 (figure 4-11, schematics section).

d. Frequency Converter A1A6A1A4. Refer to figures 1-6 and 1-15 of this section and figure 4-10, schematics section. The frequency converter generates a frequency within the 111.0 to 111.0999-MHz range. The frequency is supplied to A1A6A2A3 for generation of the variable injection frequency that is supplied to A1A2. The specific output frequency of the converter is controlled by the output of frequency/phase detector (F/ϕ DET) U1 and U2. An output frequency between 111.0-111.0999 MHz is generated by the vco, Q2. The vco control voltage to CR1 from the F/ϕ detector is a function of the phase difference between the output frequency of the oscillator and the input frequency from A1A6A1A3, both of which are applied to the F/ϕ detector, U1. The input frequency to the F/ϕ detector from A1A6A1A3, as previously noted, is determined by the bcd logic from the control. The other input frequency to the F/ϕ detector

(1.0-1.0999 MHz), representing the vco frequency, is developed in the following manner. The 111.0-111.0999-MHz vco output is applied to buffer Q6 and coupled by C36 to gate G2 of mixer Q5. The 10-MHz input from the frequency standard is applied to amplifier-buffer Q3 and coupled by C26 to X11 multiplier Q4 which provides the 110-MHz input to gate G1 of mixer Q5. The resultant output frequency, 1.0-1.0999 MHz, is supplied to squaring amplifier Q1. The 1.0-1.0999-MHz square-wave output of Q1 is applied to the input of F/ϕ detector U1A. The two frequencies are compared by the F/ϕ detector to develop a square wave pulse train at the output of U2 with a duty cycle that is a function of the phase difference between the compared frequencies. The output of U2C is applied to the low-pass filter network where the ac component is filtered out and the dc voltage becomes the vco control voltage. This is applied to varactor CR1 to vary the vco frequency as necessary to decrease the phase difference to achieve lock-on.

The +13 and +5.2 volts dc voltage is supplied by A1A4 and the +11.5 volts dc comes from A1A6A2A1 (figure 4-11, schematics section).

e. Hf Phase-Lock Loop A1A6A2A3, Variable Frequency Divider A1A6A2A2, and Voltage Regulator A1A6A2A1. Refer to figures 1-6 and 1-15 of this section, and figures 4-11, 4-12, and 4-13, schematics section. The purpose of the HFPLL is to generate a variable injection frequency within the 117 to 144.9999-MHz range for application to mixer A1A2 (figure 1-6). To accomplish this, A1A6A2A3 requires the 111.0 to 111.0999-MHz input from A1A6A1A4, the 100-kHz signal from A1A6A1A2, and the phase/lock control signals from A1A6A2A2. During locked operations (normal operating conditions with power on and all tuning complete), the frequency generating circuits of A1A6A2A3 operate independently of A1A6A2A2 and A1A6A2A1. The HFPLL (figure 4-13, schematics section) consists of the vco, Q104 and varactors CR101 and CR102; the sample and hold detector, Q3; the mixer, Z1; and the associated buffer stages for the vco and mixer output signals. The output frequency of the vco is actively controlled by the dc control voltage applied by the sample and hold phase detector to the varactors. This detector dc output is a result of the sampled output frequency of mixer Z1. Two frequencies are applied to Z1, the 111-111.0999-MHz reference frequency from A1A6A1A4 and the 117-144.9999 MHz output frequency of vco Q104, to develop an if within the 6-33.9 MHz range (4-MHz above the 2-29.9999-MHz operating frequency selected at control A2). The output of the mixer is passed through the low-pass LC filter network to the squaring amplifier circuits of Q6 and Q7 for application to the sample and hold detector stage. The 6-33.9-MHz signal is mixed with the 100-kHz input from A1A6A1A2 in the secondary of transformer T1. The resultant 6-33.9-MHz signal is rectified and filtered by the circuits of CR3 and CR4 and Q3 of A1A6A2A3. This becomes the vco dc negative feedback voltage that is applied to varactors CR101 and CR102 of A1A6A2A3. The dc voltage varies the capacitance of the varactors, raising or lowering the vco frequency as necessary to keep the phase error in the hold-in range.

The if output from Z1 is also applied from if amplifier Q7 to squaring amplifier Q5, the output of which is routed to A1A6A2A2P2-2 (figure 4-12, schematics section). During the locked condition described above, the variable divider is inoperative, therefore, the if input has no effect. However, when the radio is first turned on or a new frequency is selected at the control a reechannel logic signal is initiated by control A2. This starts a tuning cycle within the radio that includes switching (on or off) of logic 1 and +5 V dc to various circuits of A1A6A2A2. The reechannel logic ($\overline{\text{RCP STRETCH}}$) is supplied from A1A5A2P1-33 to A1A6A2A1P1-3 via A1A5A1 and chassis A1A1. When the reechannel signal is enabled at A1A6A2A1P1-3, a ground is applied to pulse stretcher circuit U2 of A1A6A2A1 resulting in conduction of squaring amplifier Q7. Conduction of Q7 establishes the following events; (1) Q4 to conduct, (2) Q5 to conduct, (3) +14V dc potential felt at switch function of A1A6A2A3, (4) Q8 ceases conduction, (5) Q9 to conduct, and (6) Q6 to conduct. The conduction of Q6 applies a ground potential on connector pin A1A6A2A1P2/A1A6A2A2P2-5 (5 V dc CONTROL line). A ground

on this pin forward biases series control switch Q2 of A1A6A2A2 thereby enabling the logic 1 and +5 V dc function. These two functions are enabled as long as control transistor Q2 is held on by the 5 Vdc CONTROL signal from A1A6A2A1. When a LOCK (LOCK=O) pulse occurs on connector pin A1A6A2A1P2-3, the 5 V dc CONTROL line is disabled and Q2 ceases conduction. This disables logic 1 and +5 V dc on A1A6A2A2.

Refer to figure 4-12, schematics section. A1A6A2A2 performs the frequency/phase discrimination and vco control functions for the hf phase-lock loop in a manner similar to those functions previously covered for A1A6A1A4. When logic 1 and +5 V dc is enabled as a result of a rechannel pulse, the variable dividers, U2-U5 of A1A6A2A2, receive the bcd logic signals from the control. The bcd logic, representing the selected frequency, is processed for comparison with the logic output of divider U1 (6-33.9 MHz), representing the HFPLL vco output frequency, to determine the frequency and phase difference with reference to the 25-kHz signal from A1A6A1A2 via A1A6A2A1. The phase difference output from the frequency/phase discriminator, U10 through U12 of A1A6A2A2, is applied to the PHASE signal line, A1A6A2A2P2-4, the duty cycle of which is a function of the phase difference between the compared frequencies.

Refer to figures 4-11, 4-12, and 4-13, schematics section. The PHASE signal at A1A6A2A2P2/A1A6A2A1P2-4 is applied to the pulse shaper transistor, A1A6A2A1Q3. The output of A1A6A2A1Q3 is applied to FET A1A6A2A3Q8 for filtering and conversion to a dc vco control voltage. The dc level, proportionate to the phase difference, is applied to the varactors to retune the vco to reduce the phase difference until lock-in is achieved. When lock-in occurs, the frequency phase discriminator of the variable divider (figure 4-12, schematics section) provides a LOCK signal at A1A6A2A2P2-3 from NOR gate A1A6A2A2U6B, which is routed to inverter A1A6A2A1U2A and coupled to the pulse shaper amplifier stage, Q7, Q4, Q8, and Q9, of voltage regulator A1A6A2A1. One output from A1A6A2A1Q4 is supplied to A1A6A2A3 (SWITCH signal) to turn off FET A1A6A2A3Q8. This transfers the control of vco A1A6A2A3Q104 from A1A6A2A2 to the sample and hold circuits of A1A6A2A3. The other output from A1A6A2A1Q4 is amplified by A1A6A2A1Q9 and applied as a cut off signal to switch transistor A1A6A2A1Q6 as previously discussed in this subsection (e).

When a frequency change is initiated at the control, the bcd logic is processed by A1A6A2A2 to provide a transmit inhibit signal (XMT INHIBIT to A1A5A2P1-22 to prevent transmission during the tune cycle of the radio. The +5.2 volts dc at A1A6A2A2-11 is supplied by A1A4.

Refer to figure 4-11, schematics section. In addition to the circuits already discussed, A1A6A2A1 provides regulating circuits for the +11.5 and +14 volts dc voltages as well as signal interface between the various synthesizer subassemblies as shown on figure 4-11. The +14-volt dc regulator consists of series regulator transistor Q1, reference voltage regulator VR1, and comparator U1B, which is connected to the output voltage divider R3, R4, and R12, and the reference voltage divider, VR1, R10, and R11. The collector of series regulator Q1 is connected to +25.2 V dc (sw and fltr). A change in the +14-volt dc output appears as a voltage change across voltage divider R3, R4, and R12. This change is compared with the reference voltage by the comparator U1B and reflected as a bias change at the base of series regulator Q1. An increase in bias reflects an increase in the output voltage. Consequently, the increased bias reduces conduction of Q1 which reduces the output voltage until +14 V dc is reached. In like manner, a decrease in bias reflects a decrease in the output voltage. This increases Q1 conduction to increase the output voltage until the +14-volt output level is reached. The +11.5-volt voltage regulator, Q2, VR3, and U1A, are connected to the reference voltage divider VR1, R10, and R11, and +11.5-volts dc divider R7, R8, and R9. The series regulator Q2, connected to +13 volts dc, and the control circuits operate in the same manner as Q1 to provide a regulated +11.5 volts dc output.

The +14- and +11.5-volt dc outputs are distributed to the various frequency synthesizer subassemblies as shown on the voltage regulator schematic diagram, figure 4-11.

1.7.4.2.2.6 Power Supply A1A4

Refer to figure 1-16 and 1-33 of this section and figure 4-4, schematics section. Power supply A1A4 provides regulated +13 volts and +5.2 volts dc outputs from a +25.2-volt dc source (battery). The routing of source voltage is shown on the power distribution diagram, figure 1-33 of this section. The +13 V dc switching regulator circuits consist of series switch transistor Q1, fly-back diode CR1, control transistors Q3, Q4, Q5, comparator transistors Q6 and Q7, and reference voltage regulator VR4. Transistor Q1 conducts in 14- to 35-usec intervals in response to bias changes effected by the comparator, Q6 and Q7. If the sampled output voltage applied to Q6 is high compared to the reference voltage applied to Q6, the series switch transistor is saturated for reduced periods of time during its operating interval by the reduced on-time of the control transistor Q3. The on-time of Q3 is reduced by the increased bias voltage from the Darlington pair of transistors, Q4 and Q5, which reflects the voltage error (high voltage) determined by the comparator Q6. During the conduction cycle of series switch Q1, the reduced current flow causes the output voltage to decrease toward the reference level until the correct output (+13 V dc) is reached. Conversely, if the output voltage decreases, the effective bias reverses to increase the conduction time of Q1 and raise the output voltage to the normal level. Transistor Q2 provides overcurrent protection for the +13 V dc regulator network.

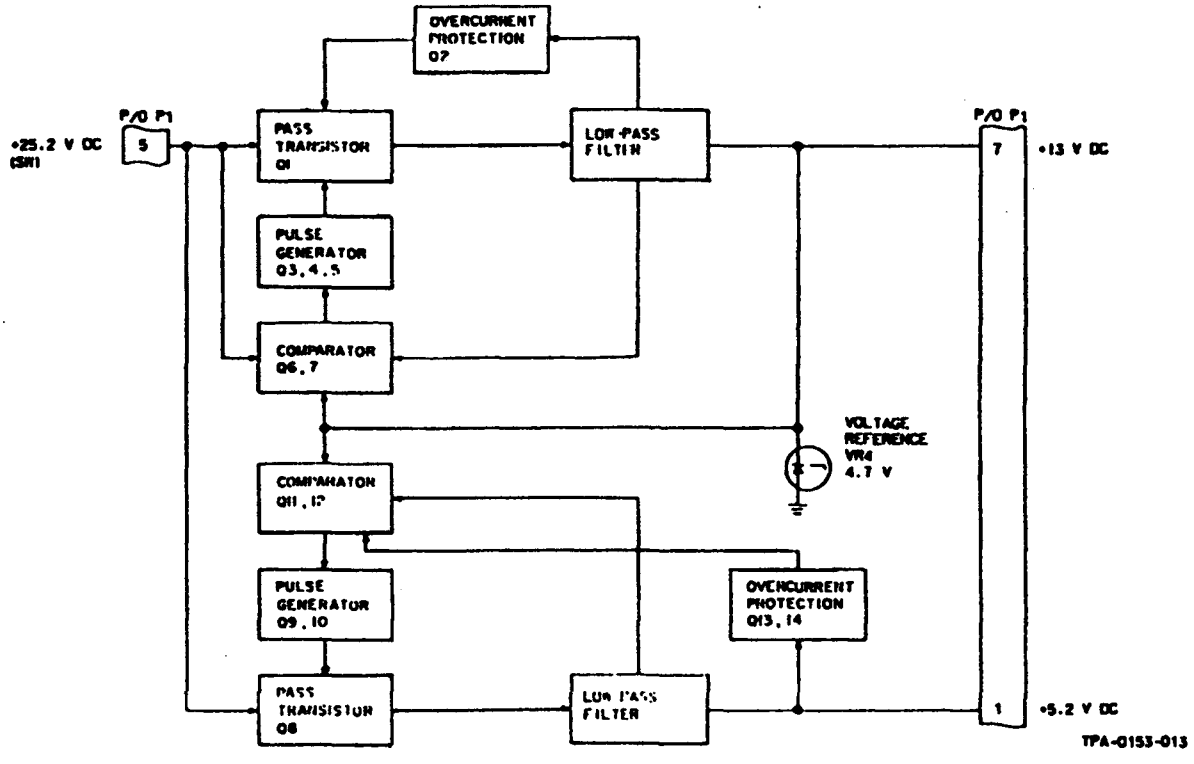


Figure 1-16. Power Supply A1A4 Simplified Schematic Diagram

The +5.2-volt dc regulator network is comprised of series switch Q8, control circuits Q9 and Q10, comparator Q11 and Q12, and reference voltage regulator VR4. The operation of the +5.2 V dc regulator is similar to the operation of the +13 V dc regulator. Transistors Q13 and Q14 provide overcurrent protection for the regulator.

1.7.4.2.2.7 Receiver-Transmitter Chassis A1A1

Refer to figure 4-1, schematics section. The receiver-transmitter chassis has eight connectors, J1 through J7 and P1, and a number of filtering capacitors. The eight connectors provide interconnection between modules A1A2 through A1A6, control A2 and amplifier-coupler A3. A dc filter circuit for +25.2 V dc (SW) is also provided. The filter circuit, Q1, capacitors C1 and C2, and resistors R1 through R3 are energized when +25.2 V dc (SW) is switched on at control A2. The +25.2 V dc (SW) turns on Q1. This results in a +25.2 V dc (SW and FLTR) output from the filter network, C1, C2, and R1 through R3, to connector J6 of A1A1. When the +25.2 V dc (SW) is switched off at control A2, transistor Q1 is turned off, cutting off the +25.2 V dc (SW and FLTR) to J6.

1.7.4.3 Amplifier-Coupler A3, AM-5280/URC

1.7.4.3.1 Transmit Theory

Refer to figure 1-17. Power amplifier A3A4 of the amplifier-coupler is a three stage push-pull class AB broadband amplifier with a minimum power gain of 23.5 dB. The amplifier is designed for a maximum required drive of 100 milliwatts, and 22-watts output. An output of 22 watts allows for antenna coupler losses, and guarantees full 20-watts output when the antenna coupler is tuned to a 50-ohm load. The power amplifier can be operated at either 20- or 2-watts output. The output level is selected by a switch on control A2.

A thermal switch in the power amplifier monitors the temperature of a heat sink. In the event a safe operating temperature is exceeded, such as by over extending the duty cycle, the ALC circuit automatically limits the output at 2 watts.

The fully automatic antenna coupler is capable of tuning an 8-foot whip and 50-ohm antennas over the 2- to 30-MHz frequency range. The coupler will also tune long wire and other whip antennas at selected frequencies. Tuning time is 4 seconds typical and 7 seconds maximum. Tuning elements include servo-driven elements (A3A7 and A3A8) that provide fine tuning and frequency band switched elements (A3A9). Elements within A3A9 are used to translate antenna impedances to within the tuning range of the servo-driven elements, A3A7 and A3A8.

1.7.4.3.1.1 Power Amplifier A3A4

Refer to figures 4-18 and 4-19, schematics section, and figure 1-17 of this section. In transmit mode, rf is applied from radio receiver-transmitter A1 to rf subassembly A3A4A1. Since the PA KEY is low and +25.2 V dc (KEYED) is enabled in transmit mode, rf is passed through contacts B2/B1 of relay A3A4A1K1 to transformer A3A4A1T1. The rf is amplified by a three stage amplifier and applied to output coax A3A4A1P1. Each of the three amplifier stages of A3A4A1 is transformer coupled to the next stage. The predriver stage consists of transistor pair Q1 and Q2, the driver stage consists of Q3 and Q4, and the final amplifier consists of Q5 and Q6. The rf is amplified to about 22 watts and coupled through transformer T6 to bias/control A3A4A2, connector J1. A bias regulator circuit on A3A4A2 provides the proper dc bias levels to coupling transformers A3A4A1T1, T2, and T3 to ensure class AB amplifier operation. The amplified rf is then passed by relay A3A4A2K1 to bandswitch A3A5.

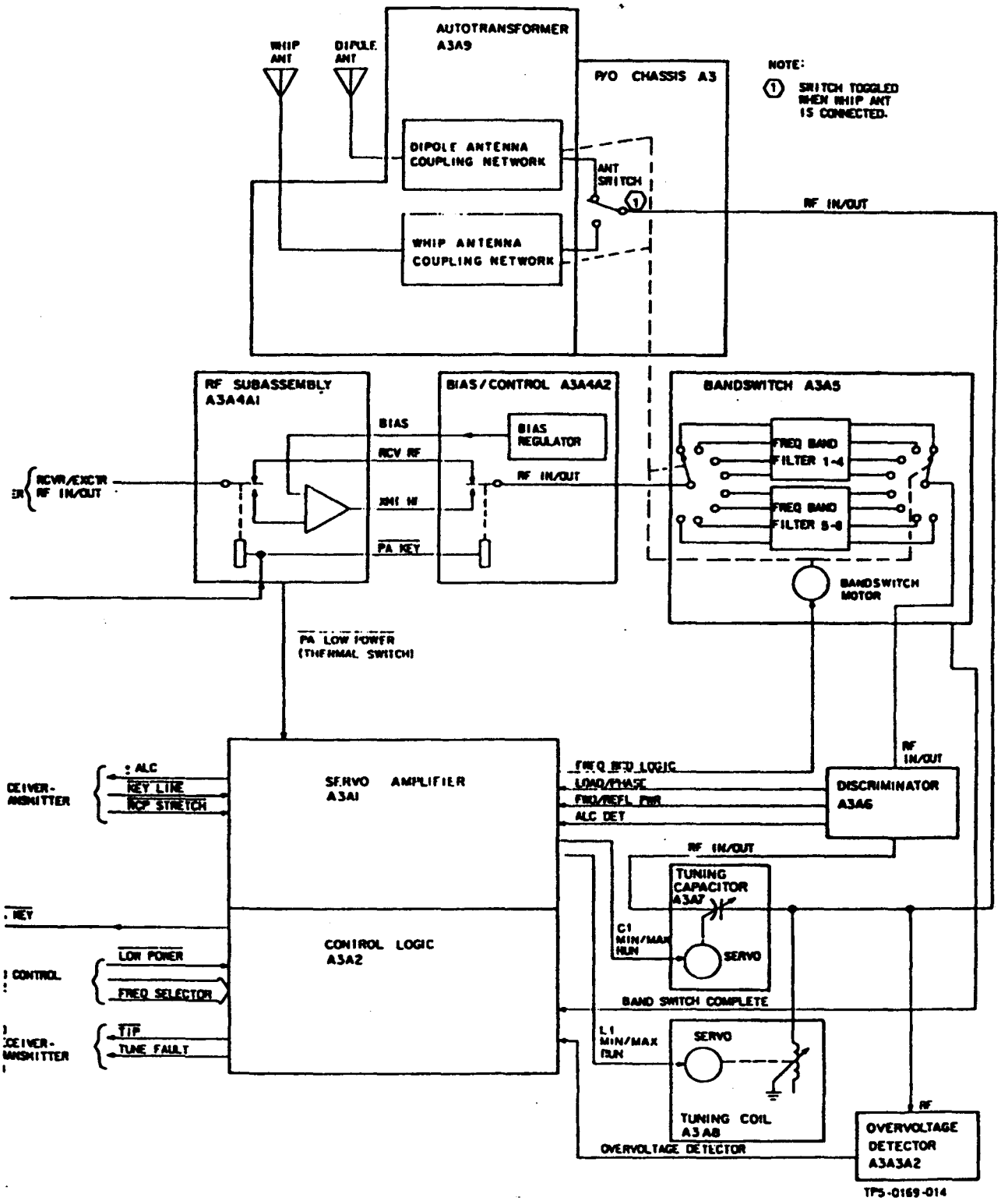


Figure 1-17. Amplifier-Coupler A3, AM-5280/URC, Block Diagram

Power amplifier ALC (automatic level control) is derived by sampling the rf drive supplied to discriminator A3A6. The resulting dc signal from the alc detector on the discriminator is fed to an op-amp on servo amplifier A3A1. The op-amp produces 0 VDC when the output of the rf amplifier is 1/2 dB or less below 20 watts and approximately -8 V dc with an rf output +1/2 dB above 20 watts.

1.7.4.3.1.2 Bandswitch A3A5

Refer to figure 1-17 this section and figure 4-20, schematics section. The bandswitch automatically selects the proper frequency band filter upon receipt of information from control logic A3A2. The band switched filters are used to provide harmonic rejection in the transmit mode. The filters are low pass filters and are selected approximately every 1/2 octave for each of the eight bands. The filter element values for each band are selected to give the best possible harmonic suppression for that band. The number of filter elements in some bands is higher than actually needed for harmonic suppression, this reduces the bandpass ripple to keep the vswr low at the higher frequencies and maintains optimum efficiency. Frequency band logic from control logic A3A2 applies a logic high to the appropriate servo band contact of switch S1. This logic high enables transistor switch A1Q2 which actuates relay A1K1 and applies +25.2 V dc to bandswitch motor B1. The motor runs and rotates switches S1, S2A, and S3 until S1 switches off of the logic high contact and opens the motor circuit. This deenergizes A1K1 and stops the motor. Simultaneously, S2A and S3 have rotated to contact positions corresponding with the activated frequency band. This connects the appropriate bandpass filter (1 of 8) to the rf signal path. The amplified rf from the power amplifier is now able to pass through S3 to the proper bandpass filter and through S2A to discriminator A3A6.

The bandswitch also drives switch S2B which applies a ground to the center tap of the variable tuning coil (A3A8) if the frequency is greater than 12 MHz. Bandswitch motor B1 is mechanically coupled to the wafer switch in autotransformer A3A9. While the motor is running the band logic selects the correct output network in A3A9. When the motor stops running (relay A1K1 deenergizes), ground is removed from the band switch complete output (A3A5P1-14). This logic output tells control logic card A3A2 that the band switching process is completed.

During the amplifier-coupler tune cycle, a logic low from the tune in progress (TIP) circuit actuates relay A1K2. This places the TIP resistor across the output (rf line) until all tuning is completed. The TIP resistor is located on A3.

1.7.4.3.1.3 Discriminator A3A6

Refer to figure 4-21, schematics section. The discriminator is a device that samples input rf power, voltage and current to the amplifier-coupler and develops dc error signals that are related to the impedance of the load and the power to the load. The loading discriminator develops a dc error voltage that is proportional to the magnitude of the impedance with respect to the normal 50-ohm impedance. The phasing discriminator develops a dc error signal that is proportional to the phase angle between the reactive and resistive portions of the load impedance. The forward and reflected power detectors are used to determine the start and completion respectively of the tuning sequence.

a. Loading Discriminator, Part of A3A6A1 and A3A6A2. Refer to figure 1-18. The loading discriminator compares the magnitude of the rf current with the rf voltage. This comparison creates an error signal output that is proportional to the difference between the impedance of the rf circuit and 50 ohms.

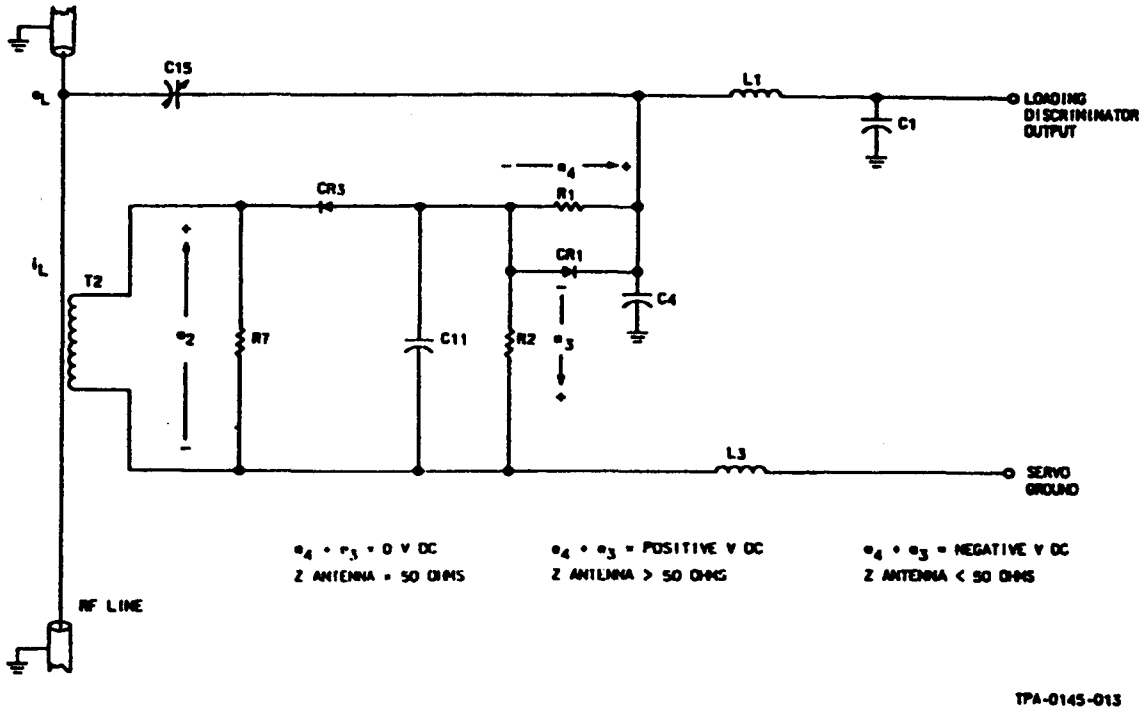


Figure 1-18. Loading Discriminator, Part of A3A6A1 and A3A6A2, Simplified Schematic Diagram

When the impedance of the rf circuit is 50 ohms, there is no error signal developed. When the rf circuit impedance is greater than 50 ohms, the error signal is positive. When the rf circuit impedance is less than 50 ohms, the error signal is negative.

Rf line current (i_1) induces a voltage (e_2) across transformer T2. When diode CR3 is forward biased, the current through resistor R2, diode CR3, and transformer T2 develops a voltage (e_3) across R2 that is proportional to the rf line current.

Line voltage is sampled by a voltage divider consisting of C15 and C4. When diode CR1 is reverse biased, the current through R1 develops a voltage (e_4) across R1 that is proportional to the rf line voltage.

C15 is factory adjusted so that the voltage across R2 is equal to the voltage across R1 when the impedance of the rf circuit is 50 ohms.

When the rf circuit impedance is less than 50 ohms, the line current increases and the line voltage tends to decrease. This causes the voltage across R2 to increase due to the increased current flow through T2. The voltage across R1 tends to decrease since it is proportional to the line voltage. The voltage difference across R2 and R1 develops

a negative error signal output. When the rf circuit impedance is greater than 50 ohms, the inverse is true, and a positive error signal is developed.

b. Phasing Discriminator, A3A6A3 and part of A3A6A1. Refer to figure 1-19. The phasing discriminator in amplifier-coupler A3 develops a dc error signal that is proportional to the phase shift between the rf voltage and the rf current. When the antenna is resistive, the line current and the line voltage are in phase, and the error signal is zero. When the antenna is capacitive, the line current leads the line voltage, and the error signal is negative. When the antenna is inductive, the line current lags the line voltage, and the error signal is positive.

The phasing discriminator is divided into two circuits. Potentiometer R5 is adjusted to balance the impedance of circuit number 1 (B, C, E, and F) and circuit number 2 (A, D, E, and F). The line voltage e_L is sampled, with no phase shift, by voltage divider C12 and C13. The induced voltage in the secondary of the transformer is 90 degrees out of phase with line current i_L. The vector addition of the induced voltage e_2 and the sampled voltage e_6 in circuit number 1 creates a resultant voltage e_4. The vector addition of induced voltage e_3 and the sampled voltage e_6 in circuit number 2 creates a resultant voltage e_5. Voltages e_4 and e_5 are rectified by CR6 and CR5 and filtered by C10 and C9. The algebraic sum of Vcc and Ved is the error output.

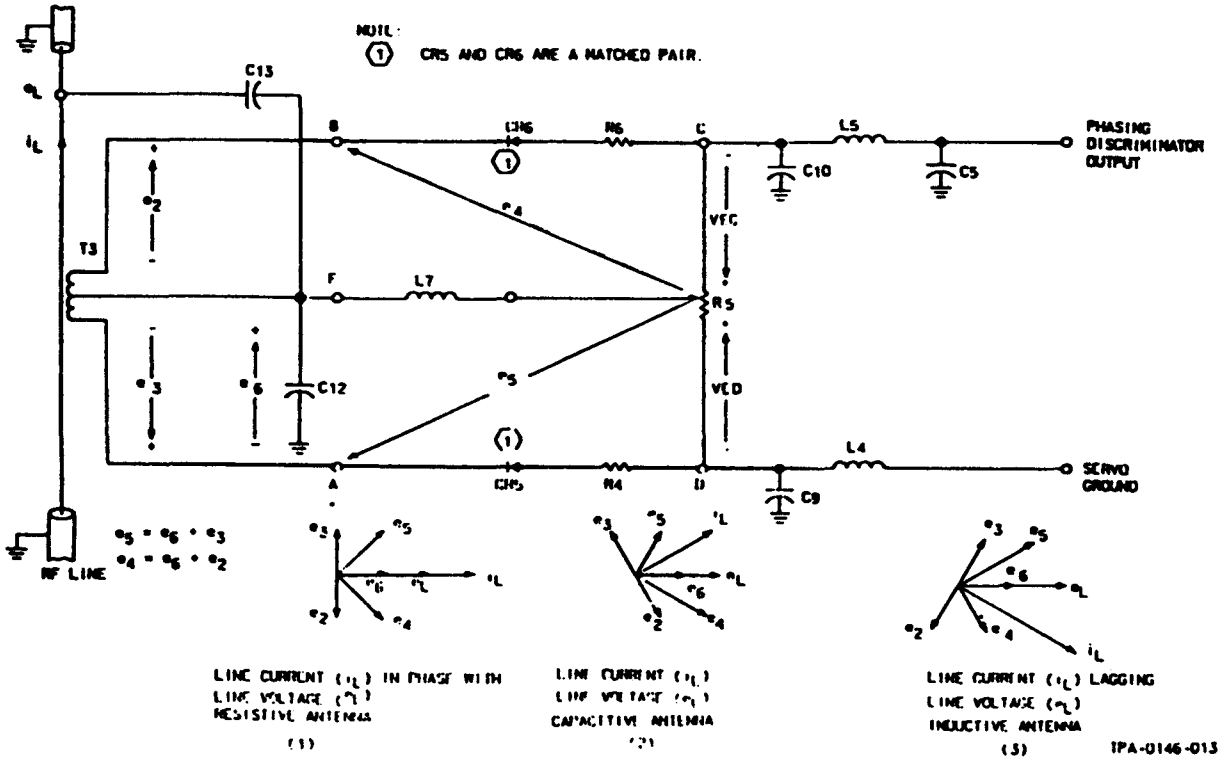


Figure 1-19. Phasing Discriminator, A3A6A3 and part of A3A6A1, Simplified Schematic Diagram

When the antenna is resistive, line current i_L and line voltage e_L are in phase. The magnitude of the resultant voltage across circuit number 1 (e_4) is equal to the magnitude of the resultant voltage across circuit number 2 (e_5); therefore, the error signal is zero (vector diagram (1) of figure 1-19).

When the antenna is capacitive, the vector addition of induced voltage e_2 and sampled voltage e_6 causes resultant voltage e_4 to increase in magnitude. The vector addition of induced voltage e_3 and sampled voltage e_6 causes resultant voltage e_5 to decrease in magnitude. The algebraic sum of resultant voltages e_4 and e_5 creates a negative error signal output (vector diagram (2) of figure 1-19).

When the antenna is inductive, the vector addition of induced voltage e_2 and sampled voltage e_6 causes resultant voltage e_4 to decrease in magnitude. The vector addition of induced voltage e_3 and sampled voltage e_6 causes resultant voltage e_5 to increase in magnitude. The algebraic sum of resultant voltages e_4 and e_5 creates a positive error signal output (vector diagram (3) of figure 1-19).

Resultant voltage e_4 is rectified by diode CR6 and then filtered by C5, L5, and C10. Resultant voltage e_5 is rectified by diode CR5 and then filtered by L4, and C9. The algebraic differences of the resultant voltages create a dc error signal output proportional to the phase difference between the rf voltage and the rf current.

Forward Power Discriminator, Part of A3A6A1 and A3A6A2. Refer to figure 1-20. The forward power discriminator generates a dc output proportional to the rf power traveling toward the antenna.

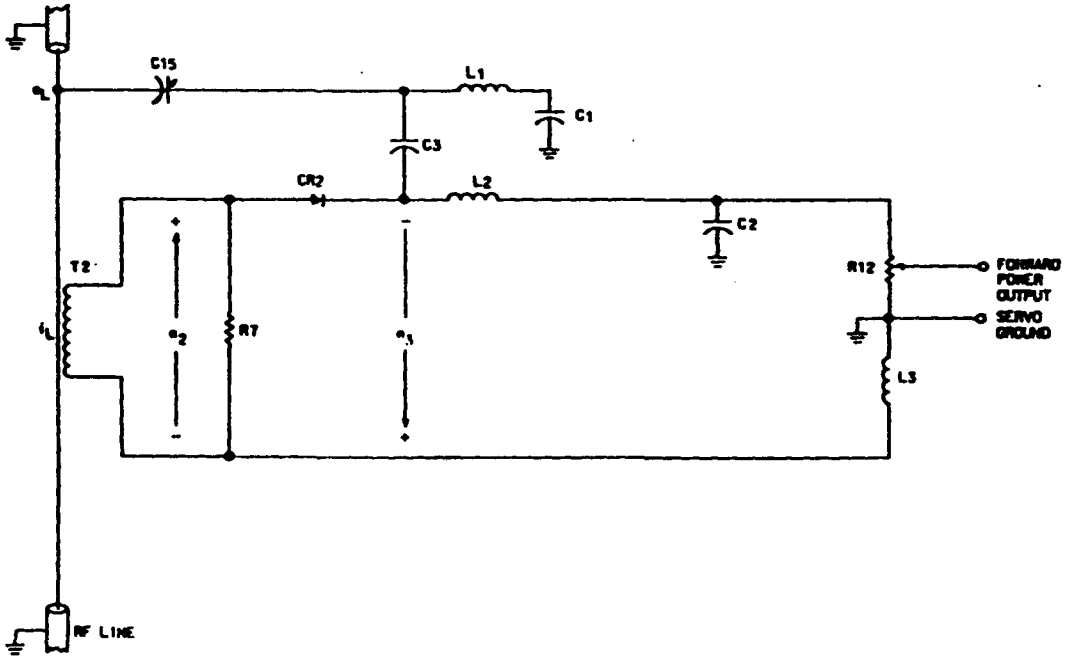


Figure 1-20. Forward Power Discriminator, Part of A3A6A1 and A3A6A2, Simplified Schematic Diagram