The secondary of transformer T2 is loaded with a low value of resistance, R7, to result in a secondary voltage (e_2) 180° out of phase with primary current. The line voltage is sampled by the voltage divider C15 and C1 and appears at the junction of CR2 and L2. The sampled portion of the line voltage is 180° out of phase with the secondary voltage across T2. On one-half of the rf cycle the induced voltage is greater in magnitude than the sampled voltage; therefore, diode CR2 is forward biased to produce a positive output when forward power is present.

d. Reflected Power Discriminator, Part of A3A6A1 and A3A6A2. Refer to figure 1-21. The reflected power discriminator develops a dc output proportional to the deviation of the vswr from 1.0 to 1. The vswr deviates from 1.0 to 1 when the antenna impedance is not 50 ohms and resistive; therefore, a reflected power output is developed when the antenna circuit is not resonant with a resistance of 50 ohms.

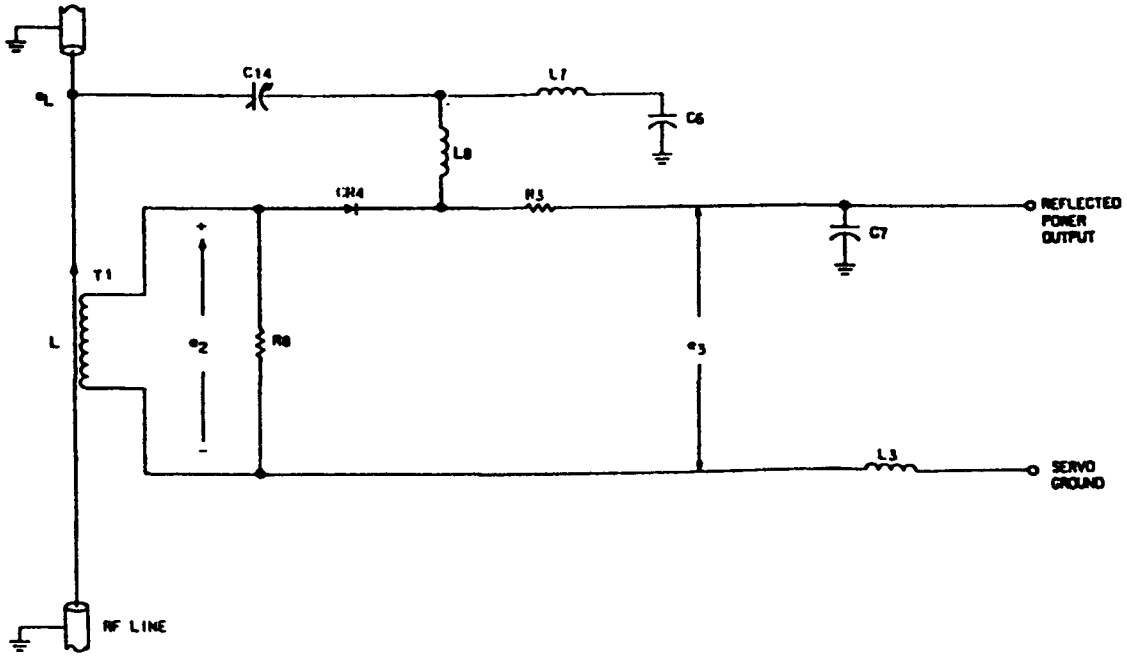


Figure 1-21. Reflected Power Discriminator, Part of A3A6A1 and A3A6A2, Simplified Schematic Diagram

The secondary of transformer T1 is loaded with a low value resistor, R8, to result in a secondary voltage (e_2) in phase with the line current i_1. The line voltage is sampled, with no phase shift, by voltage divider C14 and C6. C14 is factory adjusted to create a sampled voltage (at junction of CR4 and R3) equal to the induced voltage on T1 when the vswr is 1.0 to 1; therefore, CR4 is cut off, and there is no output.

When the antenna circuit is resonant with a resistance less than 50 ohms, the rf current increases and the rf voltage tends to decrease. The induced voltage in the secondary of T1 is greater in magnitude than the sampled voltage. Therefore, on the positive half of the rf cycle, diode CR4 is forward biased. The conduction of CR4 develops a positive output proportional to the reflected power.

When the antenna circuit is resonant with a resistance more than 50 ohms, the rf current decreases and the rf voltage tends to increase. The induced voltage e_2 is less than sampled voltage e_3. Therefore, on the negative half of the rf cycle, diode CR4 is forward biased. The conduction of CR4 develops a positive output proportional to the reflected power.

When the antenna circuit is reactive (nonresonant), the rf line voltage is out of phase with the rf line current. During a portion of each cycle, the induced voltage is more positive than the sampled voltage, and diode CR4 is forward biased. The conduction of CR4 develops a positive output proportional to the reflected power.

e. ALC Detector. The ALC detector develops a dc output proportional to the rf voltage. The rf is rectified by CR7 and referenced by zener diode VR1. The ALC detector voltage controls the output of the power amplifier during tune and low power (2 watts) modes.

1.7.4.3.1.4 Rf Tuning Network

Refer to figure 1-22 Tuning capacitor A3A7(C1) and tuning coil A3A8(L1) are servo driven elements that provide exact impedance matching to the 50-ohm output of the solid-state power amplifier. Autotransformer A3A9 contains capacitive and inductive components which are frequency bandswitched elements that translate antenna impedances to within the tuning range of C1 and L1. The inductive component, autotransformer (A3A9T1), is used exclusively for tuning the 8-foot whip antenna from 2 to 8 MHz. The antenna switch located on A3 is a mechanically interlocked switch that selects the proper tuning element in autotransformer A3A9. The switch is activated by the whip antenna. When the whip antenna is not connected, the capacitive components (A3A9C1 through C5 and C7) are automatically connected to the dipole antenna BNC connector.

a. Autotransformer A3A9. Refer to figure 1-22 in this section and to figures 4-16 and 4-24, schematics section. The autotransformer provides two frequency selective networks, one for use with a dipole antenna (capacitors C1 through C5 and C7) and one for use with a whip antenna (autotransformer T1 and capacitor C6).

The required value of capacitance (C1 through C5 and C7) is selected by bandswitch A3A5. The capacitance translates the dipole antenna impedances to within the tuning range of variable elements L1 and C1. The same is true for selecting autotransformer taps when using the whip antenna. Once antenna impedances are inside the tuning range, loading and phasing error signals run L1 and C1 to obtain the 50-ohm input impedance to the antenna.

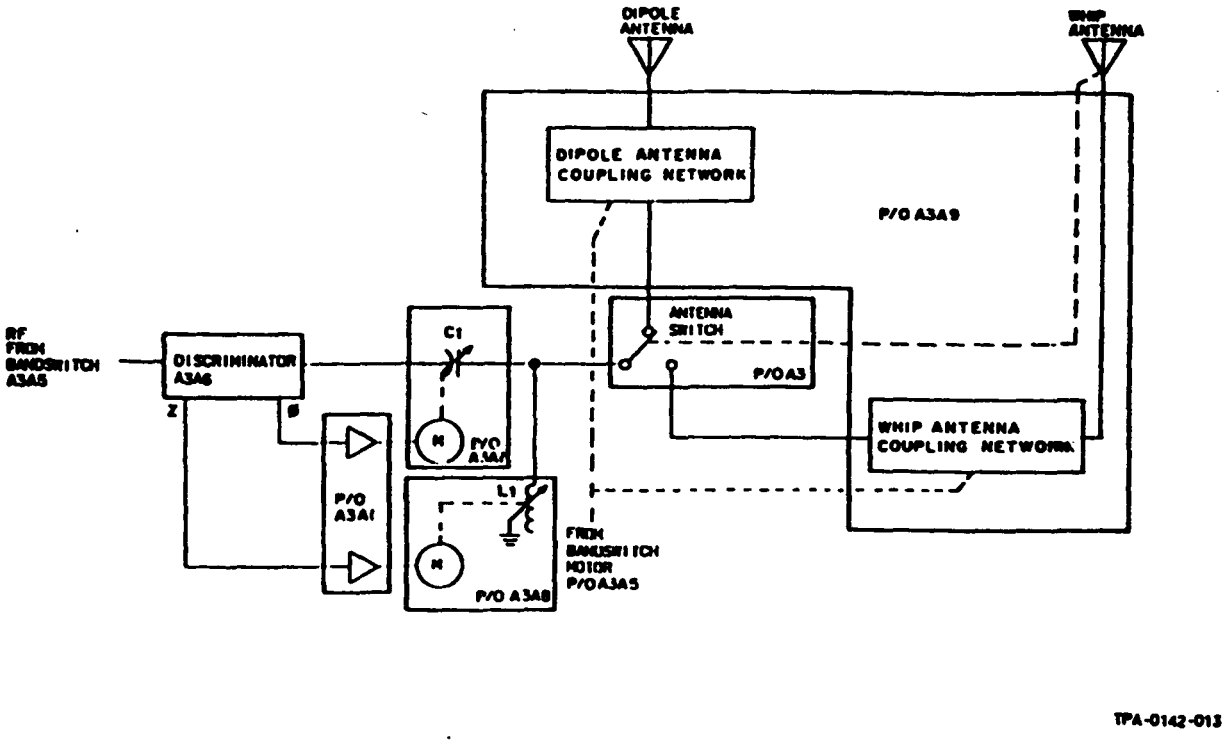


Figure 1-22. Rf Tuning Network, Simplified Schematic Diagram

Figure 1-23 shows how L1, C1, and capacitance (A3A9C1 through C5 and C7) are used to tune the antenna at one example frequency. Figure 1-24 shows the tuning procedure using the 8-foot whip antenna below 8.0 MHz. The auto transformer is switched out above 8.0 MHz.

When a whip antenna is connected, the amplifier-coupler antenna switch is mechanically switched to the normally open position. The rf is applied to switch wafers S1A and S1B of A3A9. Switch S1 is driven by bandswitch motor A3A5B1. At tuned frequencies from 2 to 7.9999 MHz, the rf is coupled through S1B to autotransformer T1. The autotransformer passes the rf through S1A to the whip antenna connector. From 8 to 23.9999 MHz, the rf is applied directly to S1A. From 24 to 29.9999 MHz, capacitor C6 provides capacitance for tuning the whip antenna.

When using the dipole antenna, the antenna switch remains in the normally closed position. The rf is applied to a contact on switch wafer S1C. Capacitors A3A9 C1 through C5 and C7 translate the antenna impedance within the tuning range of C1 and L1. The wiper arm of S1C applies the rf to the dipole antenna BNC connector.

b. Tuning Capacitor A3A7. Refer to figure 4-22, schematics section. The tuning capacitor is controlled by voltages (C1 max run and C1 min run) from servo amplifier A3A1. When a positive voltage is applied to A3A7P1-9 (C1 max run) and a ground to A3A7P1-10, current flows through the wiper arm of S1A to motor B1. Under this condition when B1 runs, the capacitance of C1 is mechanically adjusted toward maximum capacitance.

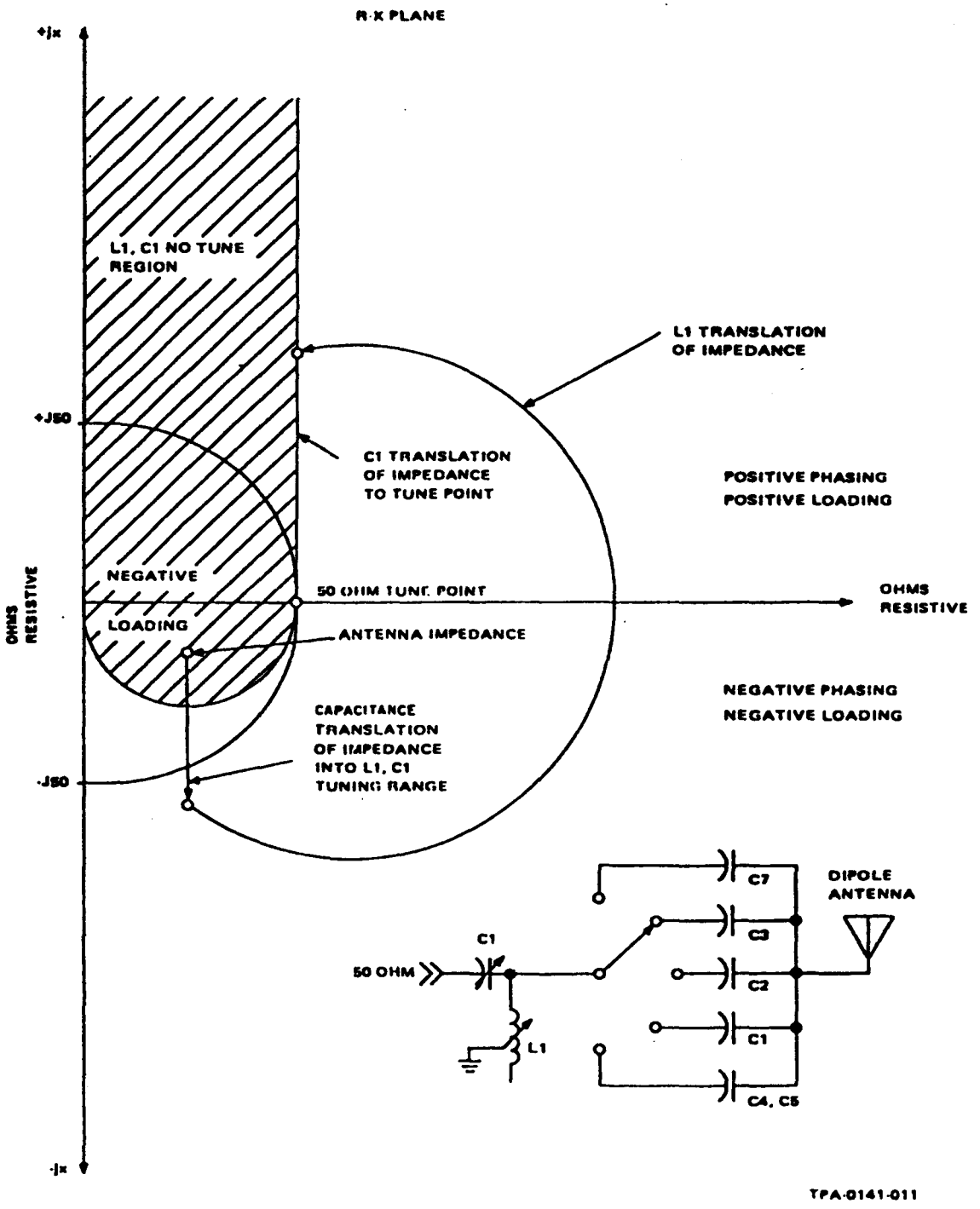


Figure 1-23. Tuning Procedure when C2 is required

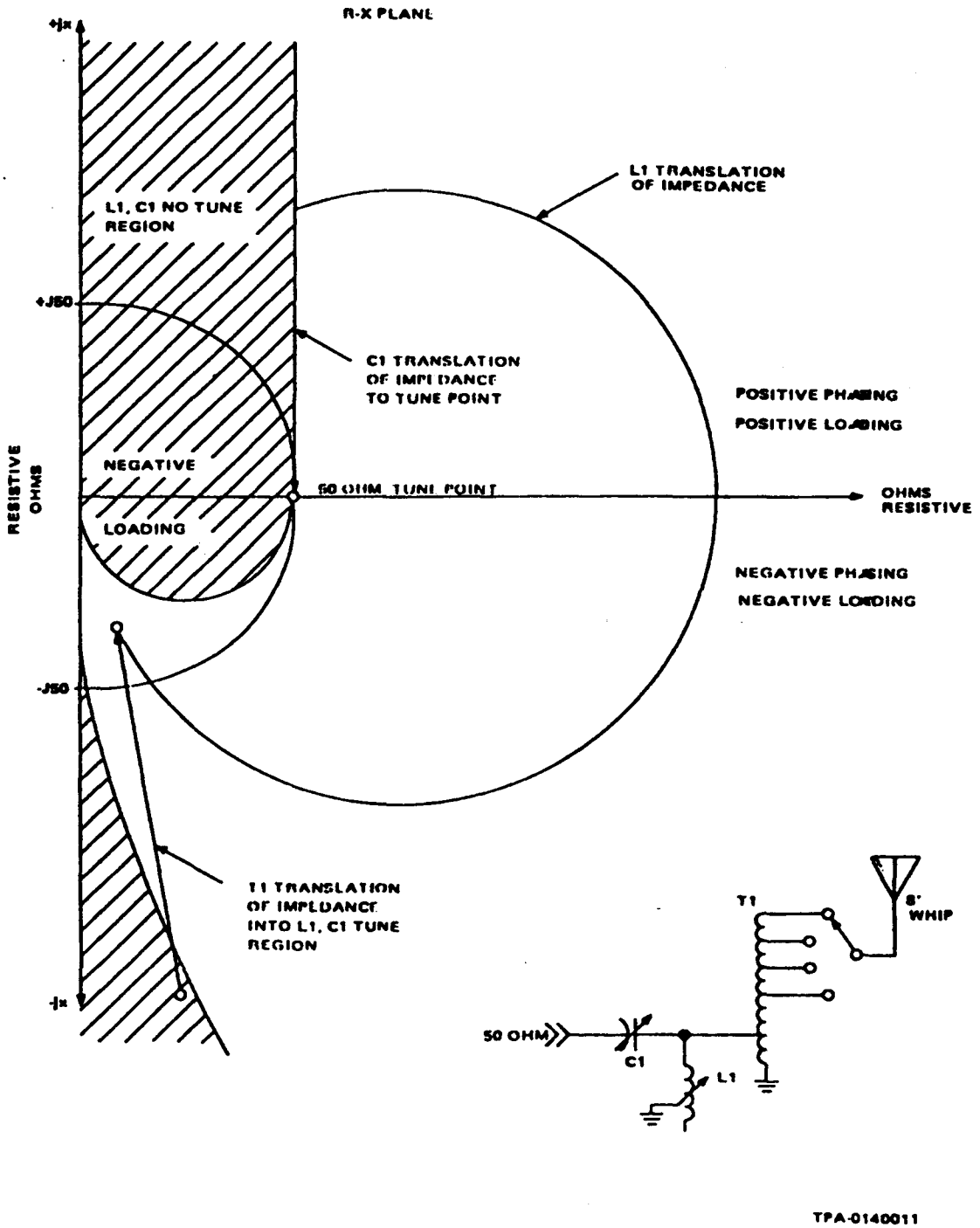


Figure 1-24. Tuning Procedure when T1 is used

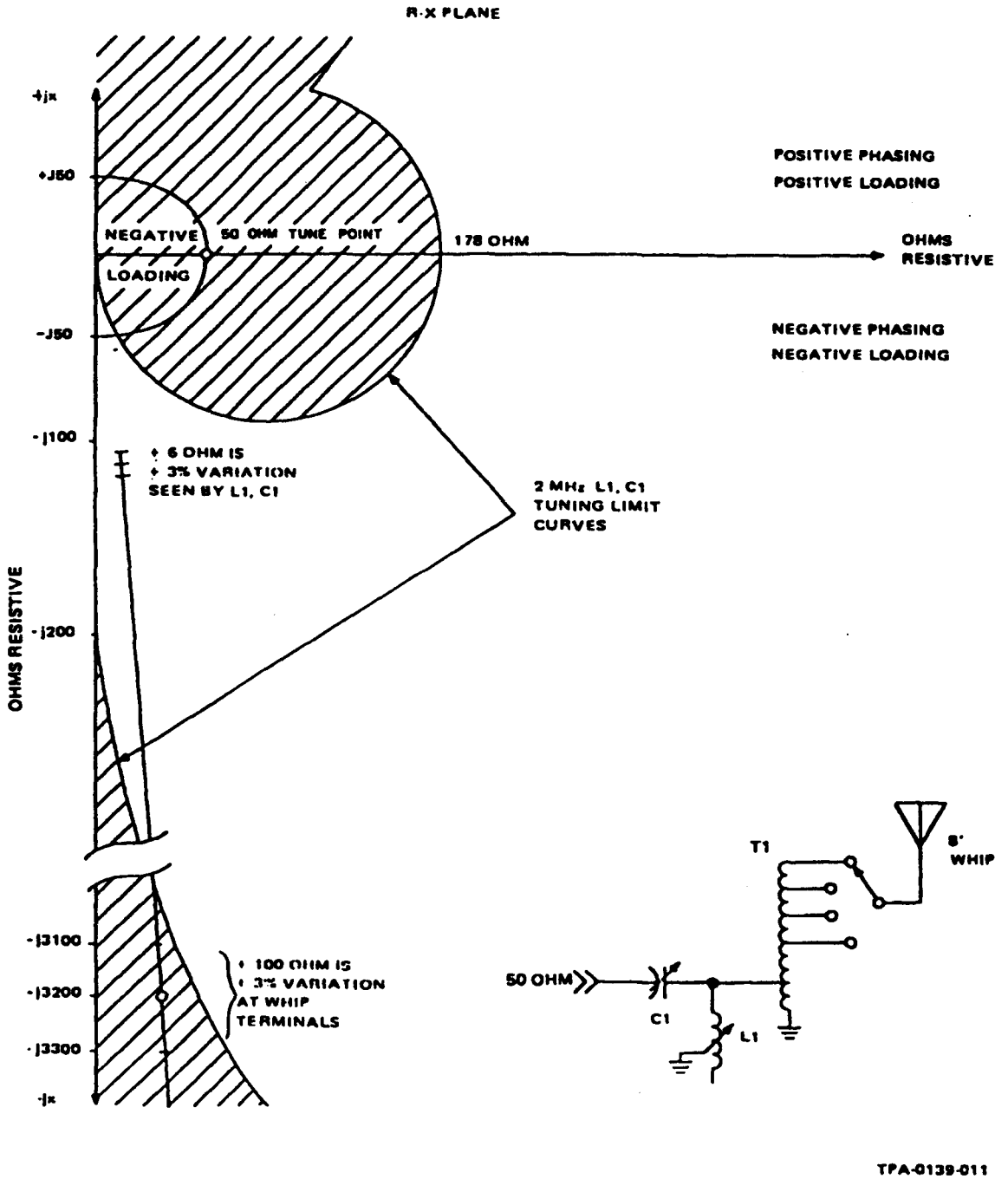


Figure 1-25. Whip Antenna Reactance Variation Reduction

S1A is mechanically connected to B1. S1A may rotate until the contact going to CR4 becomes open at maximum capacitance. When the contact opens, the voltage to B1 is removed and B1 stops. Switch S1B rotates while B1 is running. A ground established through S1B from A3A7P1-2, applies a ground at A3A7P1-5 to tell control logic A3A2 when C1 is maximum.

When a positive voltage is applied to A3A7P1-10 (C1 min run); current flows through B1 (red dot side) to the wiper arm of S1A and out through CR3. C1 max run (A3A7P1-9) is ground. B1 now runs to force C1 towards minimum and also rotates switches S1A and S1B. Switch S1A may continue to rotate until the contact going to CR3 becomes open, disabling B1. Switch S1B applies a ground to A3A7P1-6 to tell control logic A3A2 when C1 reaches a capacitance of 145 to 275 pf or less.

When logic conditions on control logic A3A2 are such that there is no forcing of the capacitor to max or min positions, the phasing voltage sample from the discriminator controls C1 position. Operation of the tuning capacitor is as discussed above, except that C1 is adjusted (toward max or min) only when a phasing voltage exists.

c. Tuning Coil A3A8. Refer to figure 4-23, schematics section. The tuning coil is positioned by L1 max run and L1 min run control voltages from servo amplifier A3A1. When a positive voltage is applied to A3A8P1-10 (L1 max run) current flows through CR1 and S1 to motor B1. L1 min run (A3A8P1-4) is ground. This condition forces B1 to run to maximum. At max inductance, the follower arm places a ground on A3A8P1-2 ($\overline{\text{L1 MAX}}$) and pulls switch S1 down to CR2. The ground at A3A8P1-2 tells control logic A3A2 that L1 is at maximum. When S1 is actuated, the current path is broken and the motor stops running. When a positive voltage is applied to A3A8P1-4 (L1 min run), current flows through servo B1, switch S2, and diode CR3. L1 max run (A3A8P1-10) is ground. This forces servo B1 to run to minimum. At minimum inductance, the follower arm places a ground on A3A8P1-9 ($\overline{\text{L1 MIN}}$) and pulls switch S2 down to CR4. The ground at A3A8P1-9 tells control A3A2 that L1 is at minimum. When S2 is actuated, the current path is broken and the motor stops running.

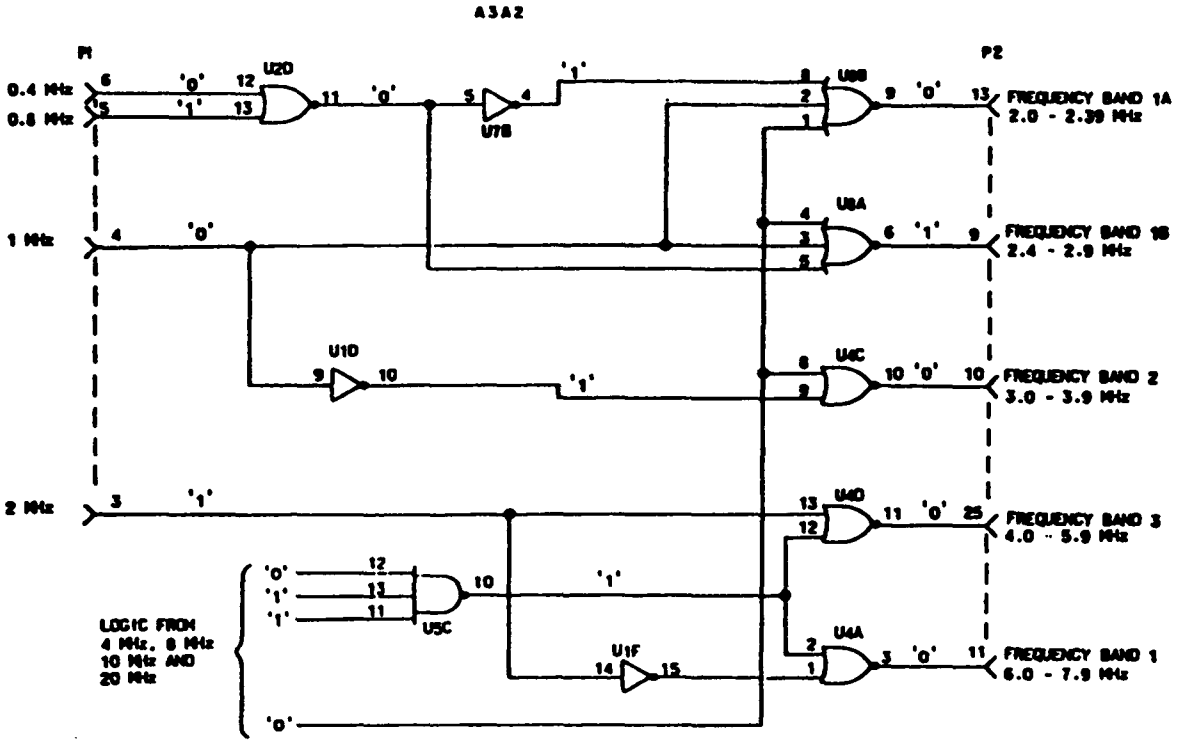
When logic conditions on control logic A3A2 are such that there is no forcing of the inductor to max or min positions, the loading voltage sample from discriminator A3A6 controls the tuning of L1. Operation of the tuning coil is as discussed above, except that L1 is adjusted (toward max or min) only when a loading voltage exists. The positive or negative voltage sample will cause L1 to run only until proper loading occurs (rf circuit impedance returns to 50 ohms).

A tab above the tuning coil is connected to the $\overline{\text{L1 Position}}$ output of A3A8. When a frequency 12 MHz or greater is selected a ground is applied by bandswitch A3A5 to the center-tap on the tuning coil L1. Should the roller make contact with the tab above 12 MHz, the ground is transferred to the $\overline{\text{L1 Position}}$ output and applied to control logic A3A2. Logic from A3A2 then disables the loading servo amplifier and the coil stops.

1.7.4.3.1.5 Control Logic A3A2

Refer to figure 4-17 schematics section. Control logic A3A2 receives binary coded decimal (bcd) frequency information, rechannel pulse (RCP STRETCH) and key line control from radio receiver-transmitter A1, servo enable from servo amplifier A3A1, and tuning coil/capacitor position logic from A3A7 and A3A8. The logic control supplies control logic signals for the amplifier-coupler, such as frequency band logic and servo command logic.

a. Frequency Decoding. Refer to figure 1-26. The bcd input from control A2 is decoded into frequency band information, see table 1-3. Band logic controls B1 on bandswitch module A3A5. High level logic is applied to the appropriate frequency line/lines on connector P1 of control logic A3A2. This logic is applied to various logic gates where



NOTE:

BCD FREQ INFORMATION FROM CONTROL = 2.8 MHz

TRUTH TABLE

NAND			NOR			INV	
A	B	C	A	B	C	A	B
0	0	1	0	0	1	0	1
1	0	1	1	0	0	1	0
0	1	1	0	1	0		
1	1	0	1	1	0		

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Figure 1-26. Frequency Band Logic, Simplified Schematic Diagram

FREQ BAND	FREQ RANGE	CONN PIN
1A	2.0 to 2.39 MHz	P2-13
1B	2.4 to 2.9 MHz	P2-9
2	3.0 to 3.9 MHz	P2-10
3	4.0 to 5.9 MHz	P2-25
4	6.0 to 7.9 MHz	P2-11
5	8.0 to 11.9 MHz	P2-28
6	12.0 to 15.9 MHz	P2-26
7	16.0 to 23.9 MHz	P2-20
8	24.0 to 29.9 MHz	P2-27

Table 1-3. Frequency Bands

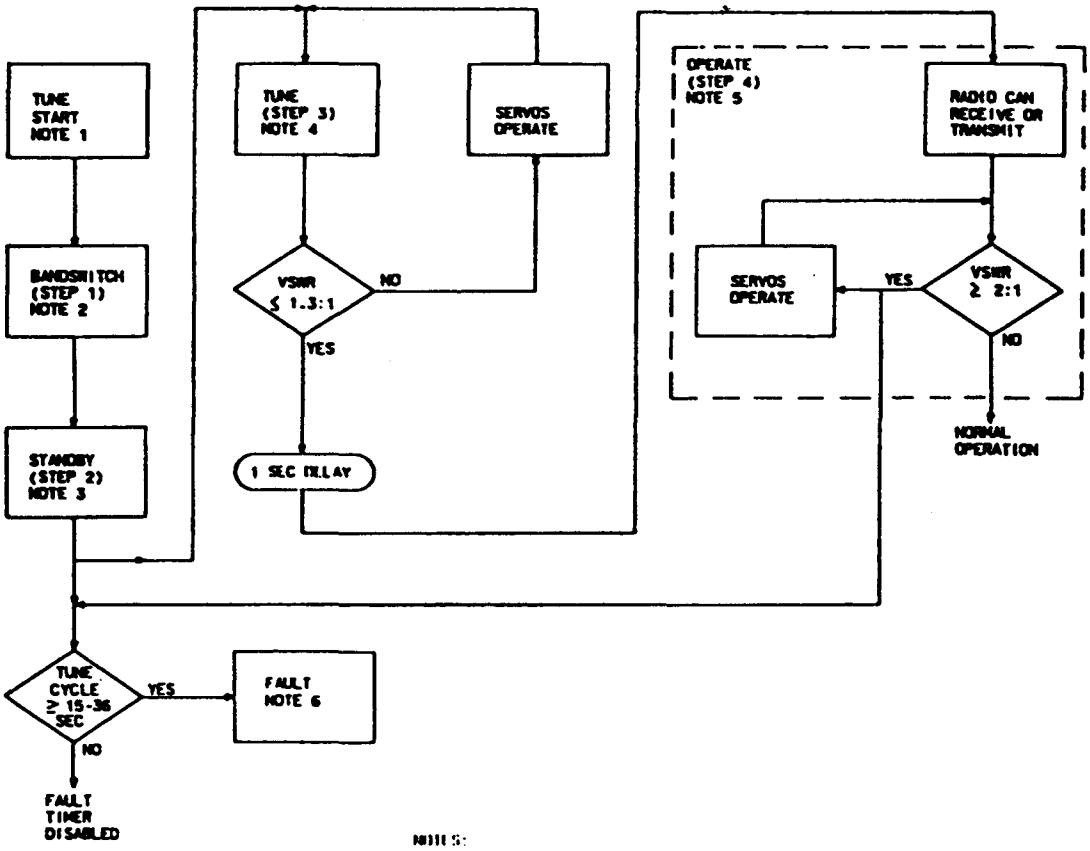
it is decoded and a logic 1 is applied to the proper connector pin on P2. This in turn enables B1 on bandswitch module A3A5. For example; assume an operating frequency of 2.8 MHz. Refer to figure 1-26. A logic 1 is applied to the 2.0 MHz and 0.8 MHz input (P1-3/5), all other frequency inputs are logic 0.

The bcd frequency logic, as shown in figure 1-26 is applied directly or indirectly through logic gates to the output gates for each frequency band. Note that output gate U8A, figure 1-26, is the only output gate with all logic 0 inputs to connector P1. Refer to the truth table in figure 1-26. A logic 1 output from U8A enables the 2.4 to 2.9 MHz frequency band (1B). All other outputs are logic 0 and the frequency bands (1A and 2 through 8) are disabled. Operation for decoding any frequency (2 to 29.9 MHz) is similar to the above example except the logic flow will change and the proper band for the selected frequency will be enabled.

At frequencies above 12 MHz, a high level logic is applied to the forcing circuits of the variable tuning elements (C1/L1) where it is used under certain conditions. This is covered in later paragraphs.

b. Tune Logic. Refer to figure 1-27. Coupler tuning is accomplished by four tuning steps (bandswitch, standby, tune, and operate) that control the logic to the servo amplifiers and ALC circuits.

Initial turn-on of primary power or the selection of a different frequency generates a rechannel pulse. The rechannel pulse sets the amplifier-coupler to tune step 1, bandswitch. The tuning sequence is illustrated in figure 1-27. A bandswitch complete signal plus coil (L1) position signal allows the logic to advance to step 2, standby. The sequence logic waits in standby for a key (key interlock) from the operator. The tuning elements are still positioned in the tuned condition for the last frequency. Upon receipt of a key (key interlock) the logic sequence goes to step 3, tune. When the tuning sequence is not in bandswitch and all bandswitching is complete, and a key interlock is



NOTES:

1. TUNE START — RECHANNEL PULSE RECEIVED WHEN POWER IS TURNED ON OR A NEW FREQUENCY IS SELECTED.
2. BANDSWITCH (STEP 1) — SWITCHED +25.2 V DC TURNED ON AND SYSTEM HELD IN UNKEYED CONDITION. BANDSWITCH COMPLETE PLUS COIL POSITION LOGIC, AMPLIFIER-COUPLER ADVANCES TO STANDBY.
3. STANDBY (STEP 2) — AMPLIFIER-COUPLER DORMANT AWAITING KEY (KEY INTERLOCK) TO ALLOW AMPLIFIER-COUPLER TO ADVANCE TO TUNE.
4. TUNE (STEP 3) — AMPLIFIER-COUPLER ELEMENTS TUNE, LEAVES TUNE AND ADVANCES TO OPERATE WHEN FWD PWR IS PRESENT AND VSWR IS LOW.
5. OPERATE (STEP 4) — KEYED OR UNKEYED, RECEIVE THROUGH A TUNED AMPLIFIFR-COUPLER IN RECEIVE, TRANSMIT WITH KEY. IF IN TRANSMIT AND SYSTEM DETECTS HIGH VSWR (2:1 FOR 1.5 SECONDS OR MORE) ELEMENTS ARE ALLOWED TO TUNE TO RESTORE LOW VSWR.
6. FAULT — TUNE FAULT IF SYSTEM DOES NOT TUNE IN ALLOTED TIME, REQUIRES NEW RECHANNEL PULSE TO RESET.

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Figure 1-27. Tune Sequence Flow Diagram

present, transistor switch Q2 applies a ground to A3A2P1-11. This ground actuates keyline relays in power amplifier A3A4 to pass the rf to bandswitch A3A5.

In tune, the following signals are used to control the tune cycle:

Servo amplifier enable	enables servos and allows elements C1 and L1 to tune
Tune-in-progress (TIP) signal to power amplifier	places power amplifier in a tune mode
TIP to radio receiver-transmitter A1	places radio receiver-transmitter A1 in a tune mode, which supplies a CW tone for tuning
Sidetone control to radio receiver-transmitter A1	rf present in receiver-transmitter A1 sidetone control circuits, which in turn generates a sidetone in the operators headset.

Forward rf power and low vswr ($\overline{\text{VSWR}}$) logic from servo amplifier A3A1 indicates that rf is present and the transmission line to the power amplifier is tuned to 50+ JO ohms to within 1.3:1 vswr. Approximately 1 second after the amplifier-coupler is tuned to 1.3:1 vswr with forward power present, the tuning sequence advances to step 4, operate. In operate, anytime the vswr indicates a mismatch of greater than approximately 2:1 for more than the allotted time delay, the servo amplifiers are enabled. The amplifier-coupler retunes until the vswr is low and the fixed delay expires, then it returns to normal operate. The vswr logic to enable the servos is delayed each time the vswr increases or decreases to provide noise immunity and allow the servos to pull-in as accurately as possible.

The tune cycle is timed by a fault circuit, see figure 1-27. If the tune cycle exceeds 15 to 36 seconds the system will fault. If a fault occurs, the tuning sequence must be reset with a tune start (rechannel) pulse.

1. Bandswitch Step. Refer to figure 1-28. The rechannel pulse ($\overline{\text{RCP STRETCH}}$) applies a 50 ms ground (logic 0) to U20D. This sets the bandswitch flip-flop (U20D and U21C). This same low level pulse is applied to U20B and resets the fault flip-flop (U20A and U20B). Simultaneously a logic 0 is gated through U14D and U15E and resets the standby, tune, and operate flip-flops. When the bandswitch flip-flop is set, the logic 1 output of U20D is applied to servo enable U9B. The output of U9B drives the circuit to energize relay A3A3A1K1. This enables +25.2 V dc (KEYED). Gate U20D also supplies a logic 1 to U21A. The logic 0 output of U21C is applied to the input of U11D. If the frequency is higher than 12 MHz and the roller on the tuning coil is contacting the L1 position tab, a logic 0 from U13D is applied to the other input of U11D. The logic 1 out of U11D enables the servo and forces the roller toward MIN until it breaks contact with the tab, at approximately mid-coil. The output of U13D changes to a logic 1 and is applied to the input of U21A. The logic 0 output of U21C is also applied to U18C to hold the power amplifier in an unkeyed condition.

   When bandswitch motor B1 on A3A5 stops running, ground is removed from the bandswitch complete circuit and a logic 1 is applied to the input of U21A. When the bandswitch flip-flop is set, bandswitch is complete, and the roller on the tuning coil is not making contact with the L1 position tab (if over 12 MHz) all inputs to U21A are logic 1. When all inputs to U21A are at logic 1, the tuning sequence advances to standby.
2. Standby Step. The logic 0 output of U21A sets standby flip-flop (U20C and U21B). The logic 0 output of U20C is applied to the input of U17C. The logic 0 output of

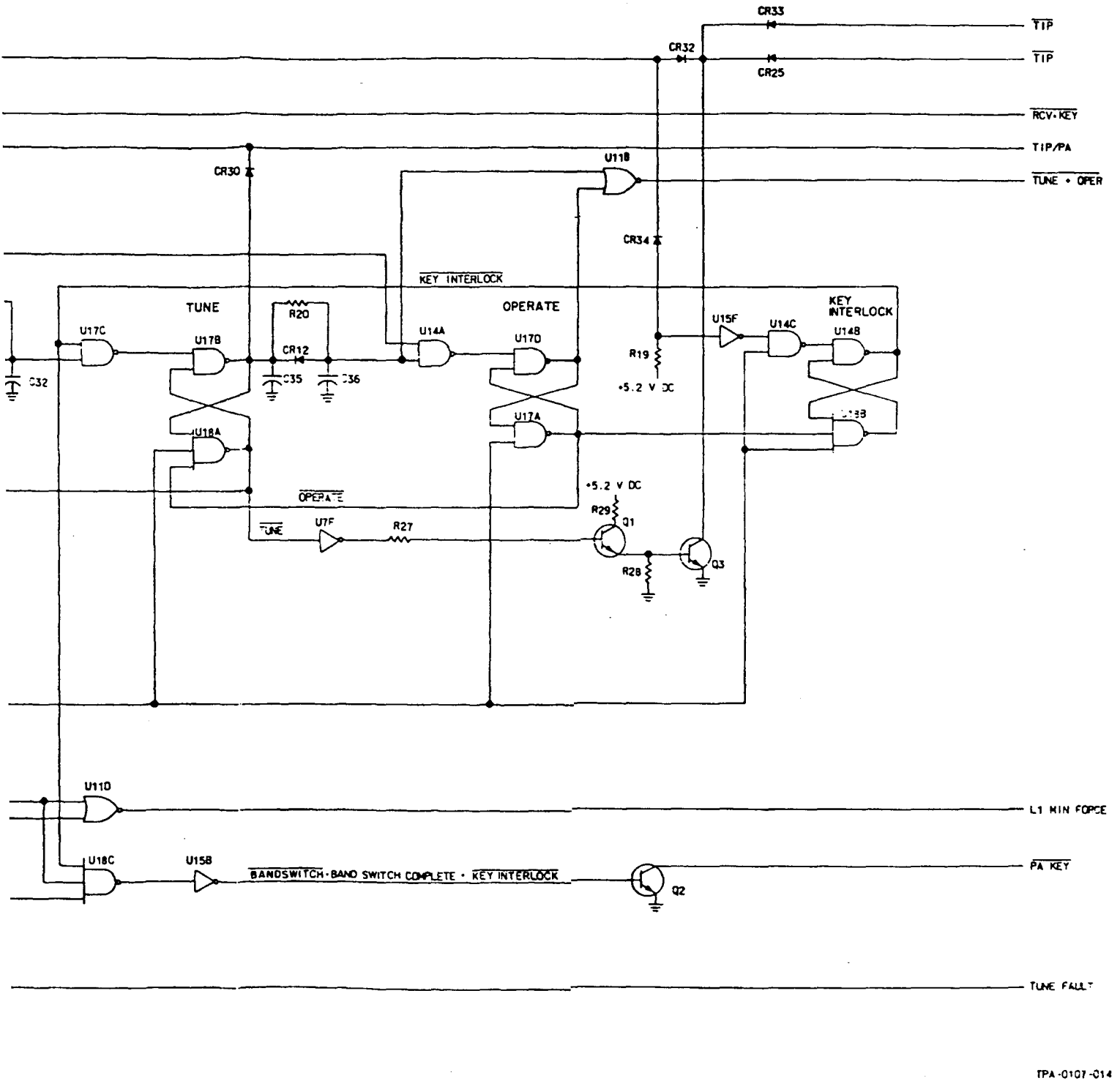

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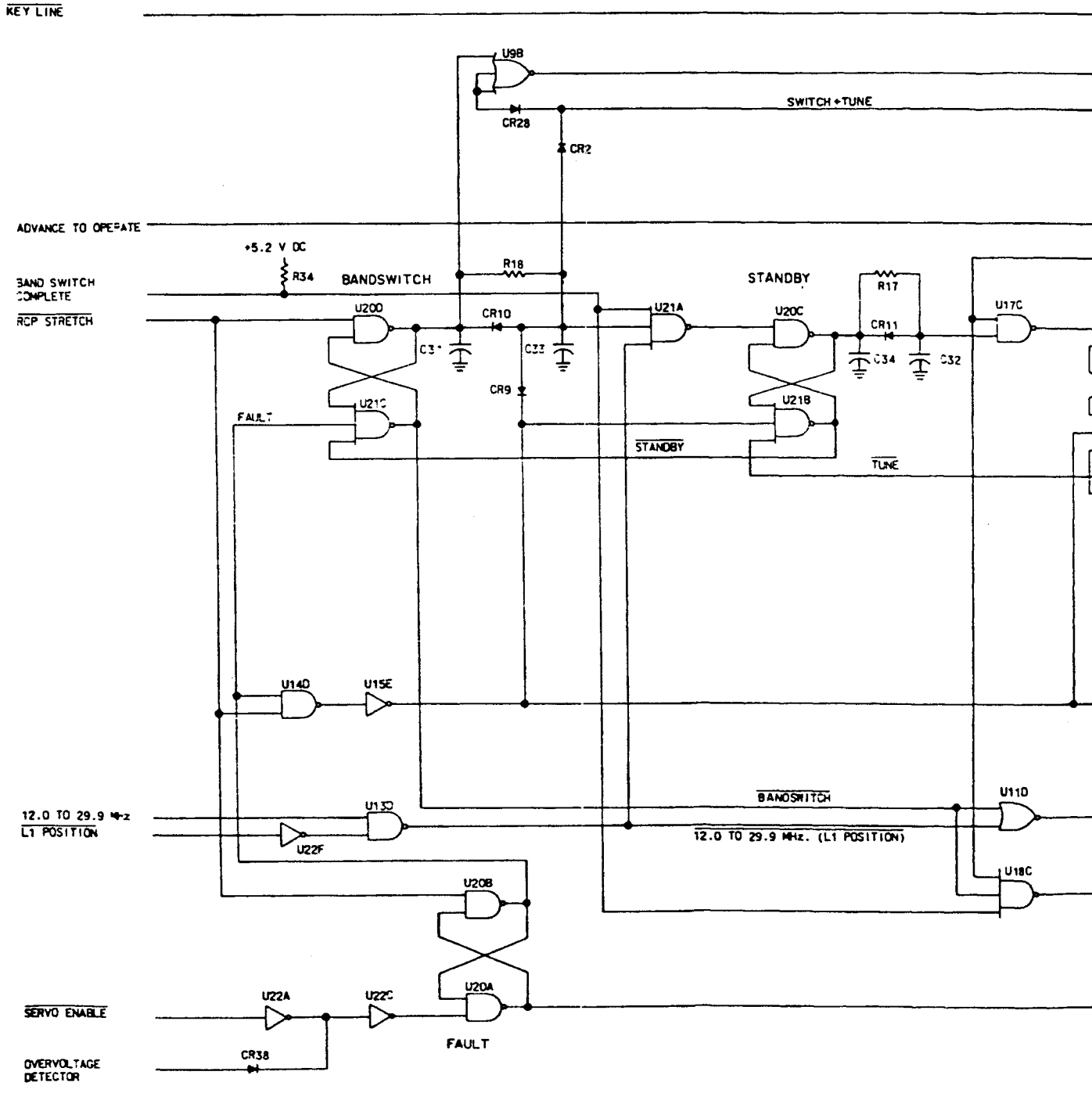
Figure 1-28. Control Logic A3A2, Simplified Schematic Diagram


KEY LINE
U9B
SWITCH+TUNE
CR28
CR2
ADVANCE TO OPERATE
+5.2 V DC
R34
BAND SWITCH COMPLETE
BANDSWITCH
R18
STANDBY
R17
RCP STRETCH
U20D
CR10
U21A
U20C
CR11
U17C
C31
C33
C34
C32
CR9
U21C
U21B
FAULT
STANDBY
TUNE
U14D
U15E
12.0 TO 29.9 MHz
L1 POSITION
U13D
U22F
BANDSWITCH
U11D
12.0 TO 29.9 MHz. (L1 POSITION)
U18C
U20B
U20A
U22A
U22C
SERVO ENABLE
FAULT
OVERVOLTAGE DETECTOR
CR38

U21B is fed back to U21C to reset the bandswitch flip-flop. In standby the radio may receive but transmission is inhibited. The tuning elements are still in their previously tuned positions unless the radio is in the RCV only mode. In the RCV only mode the tuning coil and capacitor are homed to maximum, however, the RCV only mode is used only during testing with Radio Test Set AN/PRM-501.

When the standby flip-flop is set and the radio keyed (key interlock) both inputs to U17C are logic 1. When both inputs to U17C are at logic 1 the tuning sequence advances to tune.

When a ground is applied to the keyline, a logic 0 is gated through U15F and U14C to set key interlock flip-flop U14B and U18B. The logic 1 output of U14B is applied back to the input of U17C and also to U18C to remove the power amplifier key inhibit.

3. Tune Step. When both inputs to U17C are at logic 1, the logic 0 output sets tune flip-flop U17B and U18A. The logic 1 output of U17B is applied through CR30 to enable the servos and applied through R20 to the input of U14A. The logic 0 output of U18A supplies the feedback to reset the standby flip-flop and also applies a logic 0 to U7F. The logic is inverted by U7F, amplified by Q1, and switched by Q3, placing a ground on the keyline and applying TIP logic low to radio receiver-transmitter A1. The radio receiver-transmitter turns on the rf and allows the amplifier-coupler tuning elements to tune. Discriminator A3A6 samples the rf and provides phasing and loading information to servo amplifier A3A1. A3A1 determines when the vswr is 1.3:1. When the vswr is correct and forward power is present, an advance to operate signal (logic 1) is applied to the input of U14A.

   When the tune flip-flop is set and an advance to operate logic 1 is supplied by A3A1 both inputs to U14A are at logic 1. When both inputs to U14A are at logic 1 the tuning sequence advances to step 4, operate.

4. Operate Step. The logic 0 output of U14A sets the operate flip-flop, U17D and U17A. The logic 1 output of U17D ($\overline{\text{operate}}$ or $\overline{\text{tune}}$) is applied through U11B to the L1/C1 forcing circuits. The logic 0 output from U17A is fed back to U18A to reset the tune flip-flop. This reset condition releases the hold on the keyline and TIP line applied by transistor switch Q3. In operate step, the amplifier-coupler is tuned and ready to transmit or receive as long as the vswr remains 1.3:1. Should the vswr vary, and forward power is present, the servos will be enabled until the amplifier-coupler is retuned to the correct vswr.

5. Tuning Coil/Capacitor Forcing Logic. Logic gating on control logic A3A2 determine the conditions under which the tuning elements (C1/L1) are forced to run toward maximum or minimum position. The developed forcing logic is applied to servo amplifier A3A1.

   Refer to figure 1-29. When the following logic conditions are set, C1 max forcing logic is applied to the servo amplifier forcing C1 to maximum: L1-Min, C1-Min, ($\overline{\text{12 to 29.9 MHz}}$) and (operate or tune) step. With these conditions, logic 0's are applied to the inputs of U11A and U10A. The logic 1 outputs of U11A and U10A are applied to U19B. The logic 0 output of U19B sets flip-flop U19C and U16A. The logic 1 output of U19C is applied through A3A2P3-15 to servo amplifier A3A1 which forces C1 to maximum position. If L1 runs off minimum or C1 hits maximum, the force flip-flop will reset disabling the forcing functions.

   Refer to figure 1-30. When the following logic conditions are set, L1 Max forcing logic is applied to the servo amplifier forcing L1 to maximum: L1 at Min, C1 at Max while in operate or tune. With these conditions, logic 0's are applied to the inputs of U10B and U22E. The logic 1 outputs of U10B and U22E are applied to U19A. The logic 0 output of U19A sets flip-flop U19D and U16B. The logic 1 output of U19D is applied through A3A2P3-8 to servo amplifier A3A1 which forces L1 to maximum position.

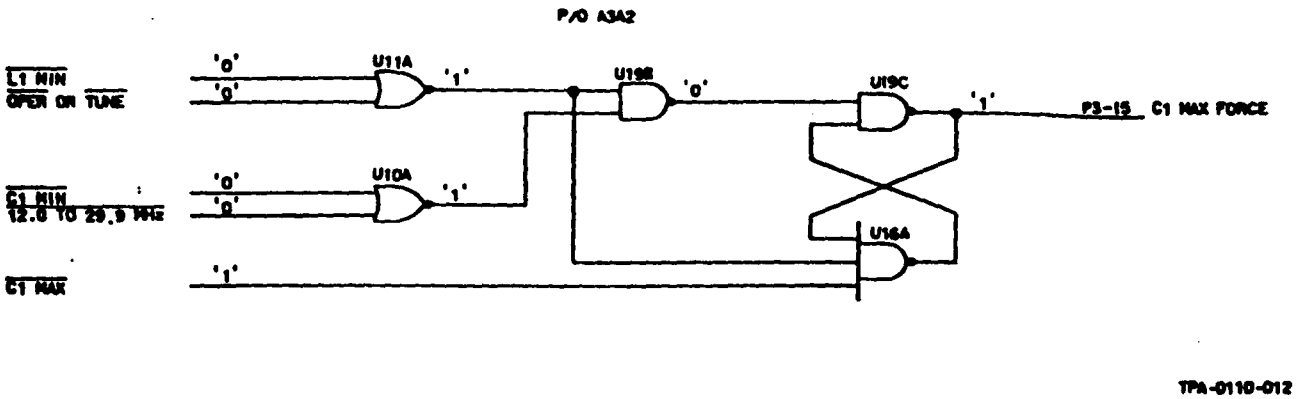


Figure 1-29. C1 Max Forcing Logic, Simplified Schematic Diagram

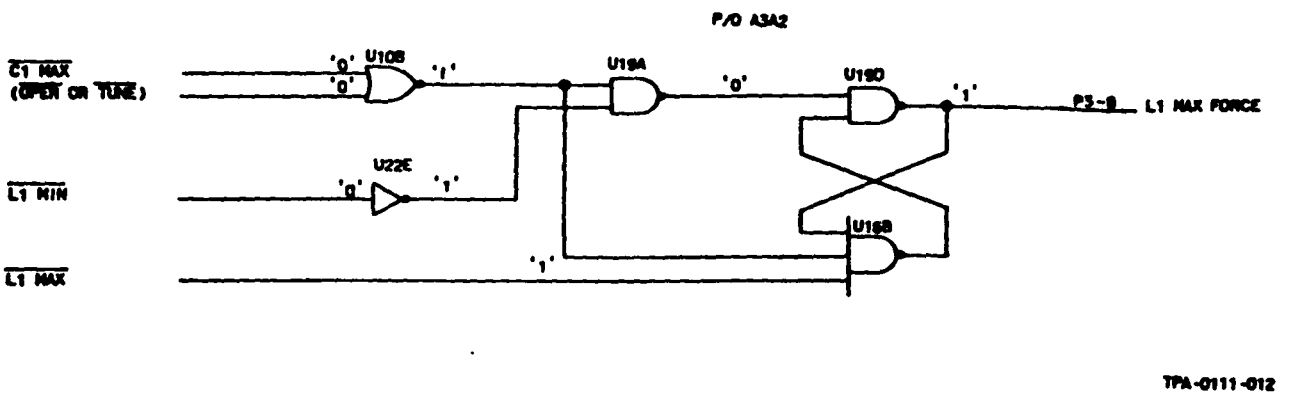


Figure 1-30. L1 Max Forcing Logic, Simplified Schematic Diagram

Refer to figure 1-31. When the following logic conditions are appropriately set, L1 Min forcing logic is applied to the servo amplifier forcing L1 toward minimum position: frequency below 12 MHz (12 to 29.9 MHz), L1 Position, L1 Max, C1 Max and (operate or tune). With these conditions, a logic 1 is inverted through U22F and applied, along with a logic 0 from the 12 to 29.9 MHz logic, to the input of U13D. The logic 1 output of U13D and a logic 0 from L1 Max are applied to U13C. Logic 0's from C1 Max and (operate or tune) are applied to the inputs of U10B. The logic 1 output of U10B and the logic 1 output of U13C are applied to the input of U13B. The logic 0 out of U13B sets flip-flop U13A and U16C. The logic 1 output of U13A is applied through A3A2P3-9 to servo amplifier A3A1 which forces L1 toward minimum position. If the frequency is above 12 MHz and L1 roller is making contact with the tab and in bandswitch tuning step, logic 0's are applied to U11D. The logic 1 output of U11D is applied through A3A2P3-9 to the servo amplifier which forces L1 toward minimum position until the roller breaks contact with the tab. Above 29 MHz the coil will force to min if C1 hits max while in the tune or operate step. The flip-flop will reset if L1 hits min or C1 comes off max or phasing sense becomes positive.

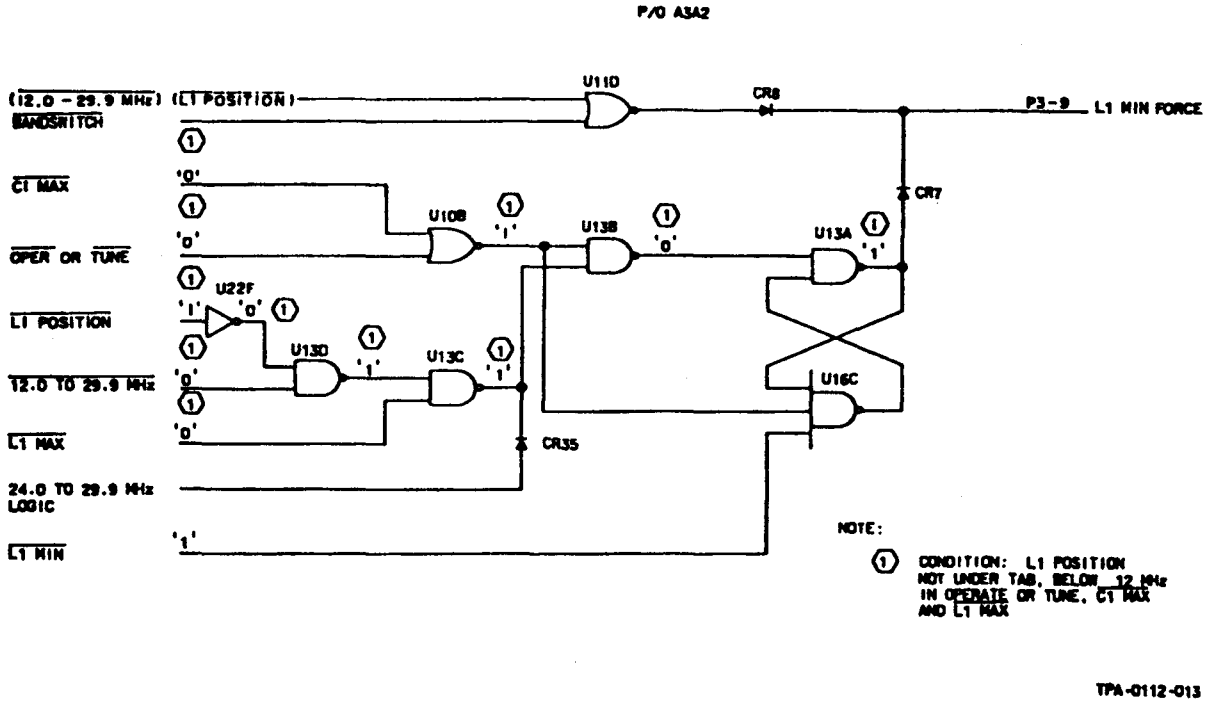


Figure 1-31. L1 Min Forcing Logic, Simplified Schematic Diagram

Positive phasing sense logic from servo amplifier A3A1 applies a logic 1 to U10B. The logic 0 output of U10B is inverted by U13B (L1 Min Force) and U19A (L1 Max Force) and resets the L1 forcing flip-flops, disabling the forcing logic and allowing the servos to control the tuning.

c. Fault Logic. Refer to figure 1-28. When the servos are enabled a logic 0 is applied by the servo amplifier to U22A in the fault circuit. The logic 0 is inverted by U22A and applied to the fault timing network. If the radio fails to tune within 15 to 36 seconds, the logic 1 is inverted by U22C and applied to the fault flip-flop, U20A and U20B. The logic 1 output of U20A (tune fault) is applied to the system. If a tune fault occurs, a logic 0 from U20B resets all the tune step flip-flops to 0 status and tuning stops. A new tune start pulse must be initiated to start a new tuning sequence. At any time the rf signal level becomes too high, overvoltage detector A3A3A2 applies a logic high through CR38 to U22C. This will also fault the tuning sequence.

Overvoltage detector A3A3A2, refer to figure 4-15 in diagrams section, provides rf sampling to protect amplifier-coupler A3 from damage due to abnormally high signal levels. The rf (approximately 850 volts peak) is sampled at the junction of the tuning coil and the tuning capacitor, and applied to A3A3A2. The rf is then filtered, rectified by CR5, and integrated by C4 to provide a normalized dc voltage to the noninverting input of U1A. A filtered 5.1 V dc is developed across zener VR1 and the inverting input of U1A. When the rectified dc voltage exceeds 5.1 volts, comparator U1A develops a positive output voltage. This positive voltage is applied to the control logic card as a fault initiate command, indicating an abnormally high level of rf.

1.7.4.3.1.6 Servo Amplifier A3A1

Refer to figure 4-17, schematics section. The servo amplifier is a dc amplifier capable of operation from a battery supply voltage of 22 to 30 V dc. The servo amplifier receives loading and phasing error voltages, forward and reflected power logic from discriminator A3A6 and forcing logic from logic control A3A2. The servo amplifier converts forcing logi and error voltages into servo drive signals to cause the tuning coil and capacitor to run towards maximum or minimum position. The servo amplifier also develops phasing sense, vswr comparison, servo controls, ALC, and sidetone voltages.

a. Tuning Coil/Capacitor Run Control. When the tuning coil forcing logic is low (both L1 max force and L1 min force), the loading sample from the discriminator A3A6 controls op amp U1A. When the loading voltage is positive (rf impedance more than 50 ohms), the output of U1A decreases, causing the output of U2B to increase, which supplies a positive voltage output at A3A1J4-4. Since U2A is now low, a ground is applied to A3A1J4-10. This forces L1 to run toward minimum. When the rf circuit impedance adjusts to 50 ohms, the loading voltage becomes zero and L1 stops running. When the loading is negative (rf impedance less than 50 ohms), the output of U1A increases, causing the output voltage of U2A to increase which supplies a positive voltage output at A3A1J4-10 to force L1 to run toward maximum. Again, when the rf circuit impedance adjusts to 50 ohms, L1 stops running. When forcing logic from A3A2 activates L1 min force or L1 max force, the forcing logic levels override the loading input. A logic '1' on the L1 min force input (A3A1J1-9) will cause a positive voltage output at A3A1J4-4 as described above. A logic 1 on the L1 max force input (A3A1J1-8) will cause a positive voltage output at A3A1J4-10, as described above. However, should the tuning coil-tab contact the roller while tuned to a frequency greater than or equal to 12 MHz, transistor Q12 is cut off. This condition back biases FET Q16 and removes Q5 and Q22 from the circuit. An open circuit appears at A3A1J4-4 which stops the tuning coil from running toward minimum.

   The phasing input from the discriminator controls op amp U1B. Logic from A3A2 applies C1 max force and C1 min force logic commands. Circuit operation is the same as that discussed above for the loading and tuning coil forcing logic.

b. Phasing Sense. The phasing input from the discriminator is applied to the noninverting input of U5B. When there is positive phasing the output of U5A develops a logic high voltage across VR8 which is applied to control logic card A3A2.

c. Vswr and Forward Power. Refer to figure 1-32. Both the forward power and the reflected power samples from discriminator A3A6 are applied to U4B. The input networks to U4B allow the forward and reflected power to be compared and a vswr check to be made. When the vswr is 1.3 to 1 a logic 1 is applied to NOR gate U6A. The logic is inverted by U6A and applied, along with logic from the forward power circuit, to U6B. (When forward power is present a logic 0 is applied to U6B.) The logic 1 output of U6B (advance to operate) is applied to control logic A3A2. Simultaneously a logic 1 is applied through a time delay network to U6D. When forward power is present, U4A applies a logic 0 to U6D. The logic 0 output of U6D, along with a logic 0 (servo enable) from A3A2 is applied to U6C. If the vswr is 1.3 to 1 and forward power is present, the output of U6C is a logic 1. The logic 1 enables transistor Q13 which in turn disables transistor Q9, removing +25.2 V dc (Keyed, filtered and enabled) thereby disabling the servo amplifiers. U6C also provides the servo enable logic to the fault circuit on A3A2. When the vswr is not 1.3 to 1 and forward power is present, a logic 0 is applied through the time delay network to U6D. The output of U6D changes to a logic 1, the output of U6C goes to a logic 0 and cuts off Q13 and allows Q9 to conduct applying +25.2 V dc (Keyed and Fltr) to servo op amps as +25 V dc (Keyed, fltr and enabled). The servos are enabled and the amplifier coupler retunes until the vswr is at the proper ratio then the tuning sequence goes back into the operate step.

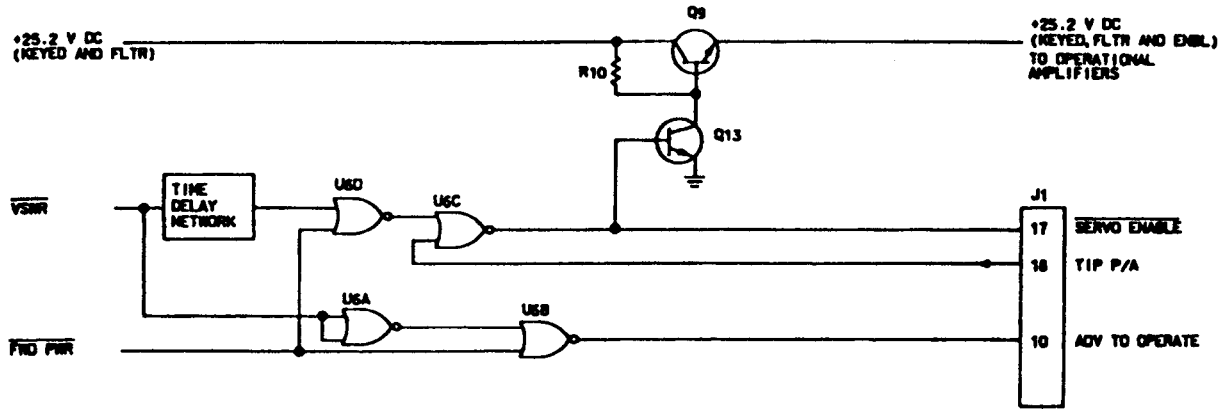


Figure 1-32. Forward Power to Vswr Comparison and Servo Enable, Simplified Schematic Diagram

d. ALC and Sidetone. In the tune mode (tune step 3) the detected ALC voltage from the discriminator controls the ALC output voltage from U5B. The cathodes of CR3 and CR1 are grounded by TIP. This disables the bias supplied through R37 and enables Q17. The ALC detector voltage from the Q17 is much higher than the forward power voltage supplied from the discriminator. As a result the ALC detector controls U5B. However, if the reflected power is too high, resistor R82 will feed bias to U5B and the forward power will be decreased.

In operate, Q17 is biased off and the output of U5B is controlled by forward power. The cathodes of CR1 and CR3 are no longer grounded. If low power is requested (P1-19 grounded) Q17 will turn on and the ALC detector will control the output of U5B.

Sidetone enabling is controlled by current summing op amp U5B. The sidetone (A3A1P1-25) is applied during tune and operate when rf is present. Five current sources feed the inverting input. When the current through R82 (reflected power) plus the current through R6 (forward power plus the current through Q17 (ALC)) is equal to the current through R33 (reference) plus the current through R36 (drive), the output of U5B goes negative. This condition turns Q10 on and applies a logic 0 to A3A1P1-25 (RF POWER) to activate the sidetone.

The servo amplifier also contains an internal -12 V dc supply circuit. Inverters U7A and U7B are tuned by R70 and C39 to develop a 20 kHz square wave. The square wave switches Q11, Q26, and Q14 on and off and controls the biasing of CR11. Zener diodes VR4 and VR5 then develop -12.4 V dc at the base of Q15, causing Q15 to conduct and -12 V dc to develop at the emitter lead.

1.7.4.3.2 Receive Theory

The following paragraphs contain a description of the rf signal path from the antenna to radio receiver-transmitter A1. For more detail on any particular module, card, or sub-assembly refer to the description of the transmit path, paragraph 1.7.4.3.1.

When using a dipole antenna, the received rf is coupled through autotransformer A3A9 wafer switch section S1C, and through its associated capacitive network to the antenna switch. When using a whip antenna, the received rf is coupled through autotransformer A3A9 wafer switch section S1A and either capacitor C6, autotransformer T1 and S1B, or directly to the antenna switch. Autotransformer T1 is used for frequencies from 2 to 7.9999 MHz only and capacitor C6 is used for frequencies from 16 to 23.9999 MHz only. The antenna switch is toggled when the whip antenna is connected.

The rf signal from the antenna switch is applied to tuning coil A3A8L1, tuning capacitor A3A7C1, and overvoltage detector A3A3A2. The tuning coil and tuning capacitor are tuned to optimum receive conditions by logic applied by servo amplifier A3A1 and control logic A3A2. Optimum receive conditions occur when the control logic is in the standby step of the tuning sequence. The overvoltage detector provides a fault initiate signal to A3A2 should the rf signal get too high.

The rf is then coupled through the discriminator to bandswitch A3A5. The bandswitch module contains two filter boards, each having four bandpass filters. The appropriate filter is selected by the bandswitch step of the tuning sequence. The band filtered rf is then applied to the power amplifier.

Relay A3A4A2K2 is deenergized when receiving. The received rf is passed to rf assembly A3A4A1. Relay A3A4A1K1 is also deenergized when receiving. The received rf is then passed through the relay to receiver-transmitter A1.

1.7.4.4 DC Power Distribution

Refer to figure 1-33. The receiver-transmitter group operates from a 25.2-volt (+5, -3 V dc) battery connected to A3J2. Four terms are used to functionally label the 25.2 volts dc shown on figure 1-33.

+25.2 V dc	voltage applied to the receiver-transmitter group when the battery is connected.
+25.2 V dc (keyed)	voltage applied when the receiver-transmitter group is keyed.
+25.2 V dc (SW)	voltage applied when switched on at the control.
+25.2 V dc (SW and filtered)	switched voltage filtered by the circuits discussed in paragraph 1.7.4.2.5.

The +25.2 volt dc battery voltage is applied from connector A3J2-1 to fuse A3A3A1F1. From the fuse, the +25.2 V dc voltage is routed to relay A3A3A1K1, A3J1-24 and -30, and A3A3A1J1-21 for distribution. When A3A3A1K1 is energized by keying the equipment, +25.2 V dc (KEYED) voltage is supplied to A3A1P1-13, A3A2P1-13, A3A4A1J1-3 and A3A4A2P1-3.

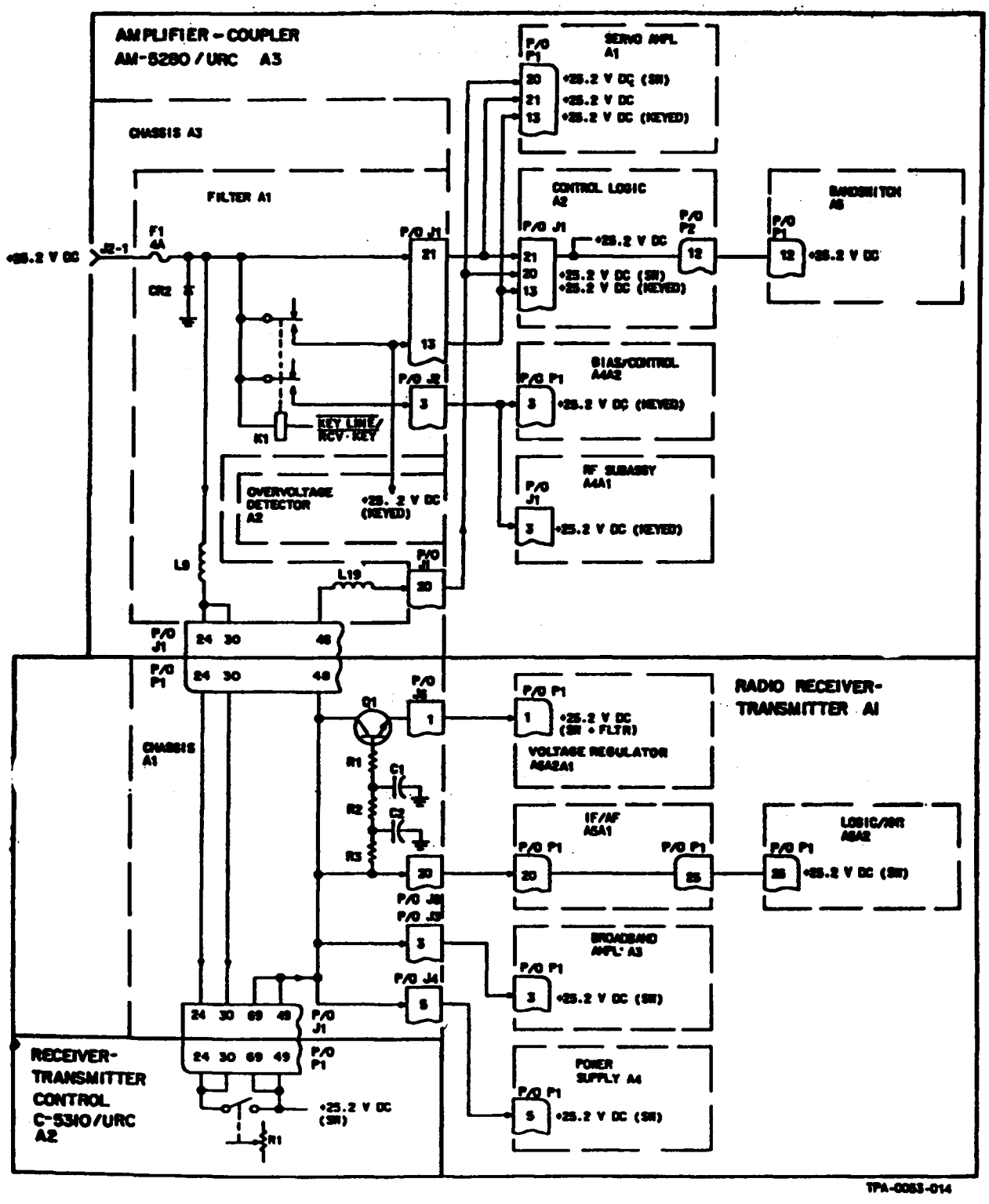


Figure 1-33. Receiver-Transmitter Group OR-5007/URC, DC Power Distribution Diagram

The +25-volt voltage is distributed to A3A1, A3A2 and A3A5, and is connected to the O section of A2R1 through connectors A3J1/A1A1P1-24, -30 and A1A1J1/A2P1-24, 30. W the receiver-transmitter group is turned on at the control, the +25.2 volts dc becomes +25.2 V DC (SW) which is applied to A2P1/A1A1J1-36, -49 for distribution (figure 1-33 The switched dc output of A1A1Q1 becomes +25.2 V DC (SW AND FLTR) and is applied to A1A6.

The +25.2 DC (SW) is applied to A1A4P1-5 and converted to regulated +5.2 and +13 volt +5.2 V DC is applied to A1A4P1 -1 and +13 V DC to A1A4P1-7 for distribution.

1.7.5 Direct Current Generator G-5002/PRC-515 Detailed Theory

Refer to figure 4-28, schematics section. The generator consists of a crank generator, a voltage regulator circuit, and a current output indicator circuit. The dc output of the hand crank generator is applied through the CR1-CR4 bridge circuit to a series voltage regulator, Q1, Q2, and Q4. Primary current flow is through series transistor Q1, curr sensing resistor R1, and diode CR5. Diode CR5 prevents battery discharge back throug the generator when it is not being operated.

For low input voltage levels (slow cranking speeds), drive transistor Q2 and series tran tor Q1 are on (control transistor Q4 is in cutoff) and the output voltage follows the input voltage. Output voltage is fed back through the voltage divider R7 and R8 to the base of control transistor Q4. VR2 is the threshold reference diode that allows Q4 to turn on wh the voltage across R9 is equal to Q4 emitter-base drop plus 5.1 volts.

When the output voltage reaches approximately +30 V dc, base drive supplied by voltage divider R7 and R9 is sufficient to turn on Q4. The conduction by Q4 diverts base drive away from Q2. Q2 and Q1 conduct less, Q1 collector to emitter voltage increases, and the output voltage is maintained at approximately 30 V dc.

The green (DS1) and red (DS2) crank speed indicator lamps are controlled by a current sensing circuit made up of R1, Q3, Q5, Q6, and VR1 and VR3. As output current increas the voltage drop across current sensing resistor R1 also increases. The voltage drop across R1, which is in the Q3 base to emitter path, controls current flow through Q3. Wi an output current flow of between 40 and 150 mA, there is sufficient current flow through Q3 to cause Q5 to turn on and light lamp DS1. With an output current of between 150 and 300 mA, there is sufficient current flow through Q3 to cause Q6 to turn on and light lamp DS2.

Missing pages:

SECTION II: Maintenance

SECTION III: Parts List

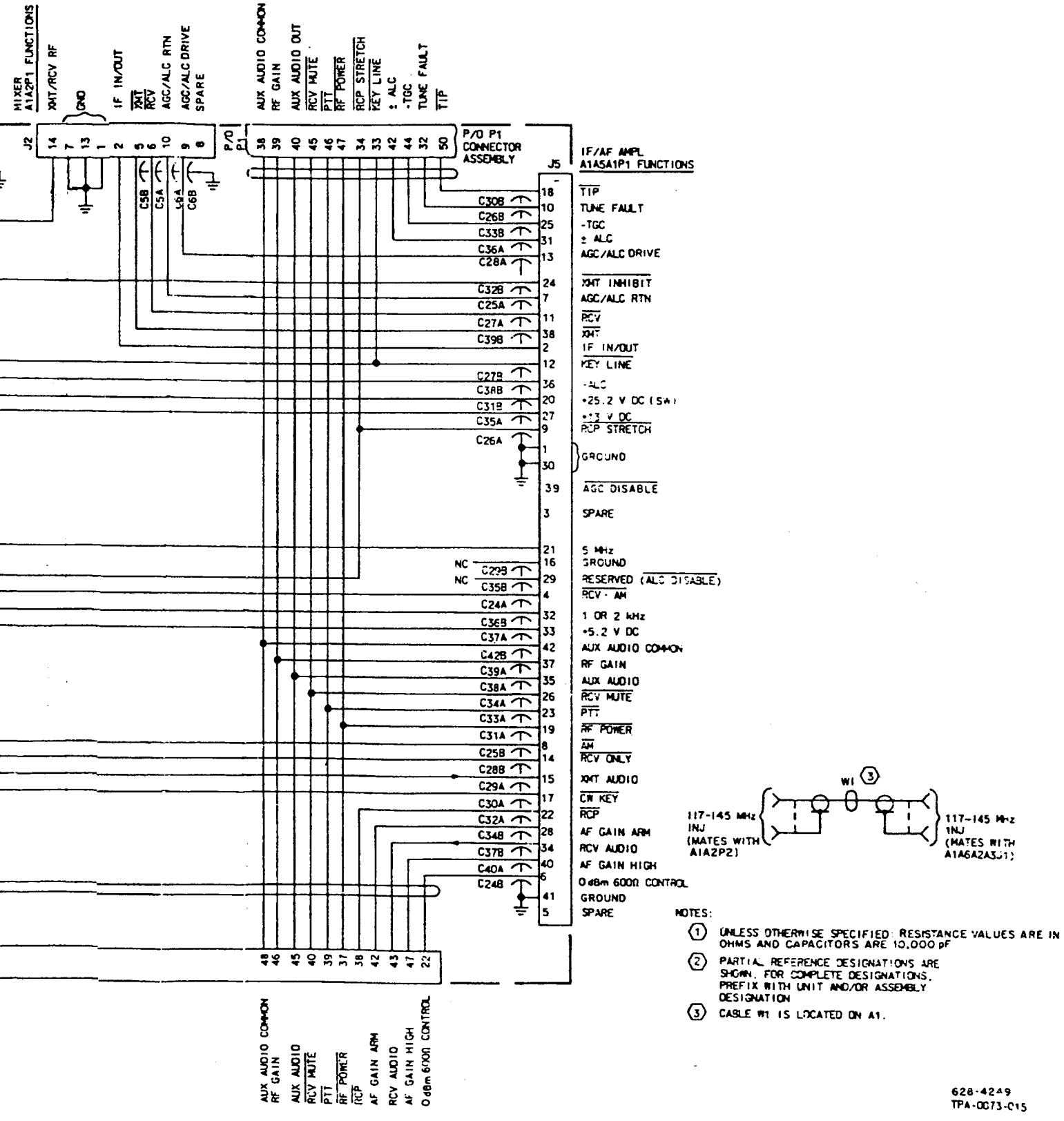
SECTION IV

SCHEMATICS

4.1 GENERAL

Schematic diagrams are included for Receiver-Transmitter Group OR-5007/URC, Handset H-5017/PRC-515, Handset-Microphone H-5016/PRC-515, Electrical Power Cable Assembly CX-5229/PRC-515, and Direct Current Generator G-5002/PRC-515. The schematic diagram titles and figure numbers are:

FIGURE	TITLE
4-1	Chassis A1A1, Schematic Diagram
4-2	Mixer A1A2, Schematic Diagram
4-3	Broadband Amplifier A1A3, Schematic Diagram
4-4	Power Supply A1A4, Schematic Diagram
4-5	If/Af A1A5A1, Schematic Diagram
4-6	Logic/Tx A1A5A2, Schematic Diagram
4-7	Frequency Standard A1A6A1A1, Schematic Diagram
4-8	Fixed Frequency Divider A1A6A1A2, Schematic Diagram
4-9	Lf Phase-Lock Loop A1A6A1A3, Schematic Diagram
4-10	Frequency Converter A1A6A1A4, Schematic Diagram
4-11	Voltage Regulator A1A6A2A1, Schematic Diagram
4-12	Variable Frequency Divider A1A6A2A2, Schematic Diagram
4-13	Hf Phase-Lock Loop A1A6A2A3, Schematic Diagram
4-14	Receiver-Transmitter Control A2, C-5310/URC, Schematic Diagram
4-15	Amplifier-Coupler A3, AM-5280/URC, Schematic Diagram
4-16	Servo Amplifier A3A1, Schematic Diagram
4-17	Control Logic A3A2, Schematic Diagram
4-18	RF Subassembly A3A4A1, Schematic Diagram
4-19	Bias/Control A3A4A2, Schematic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS AND CAPACITORS ARE 10,000 pF
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION
3. CABLE W1 IS LOCATED ON A1.

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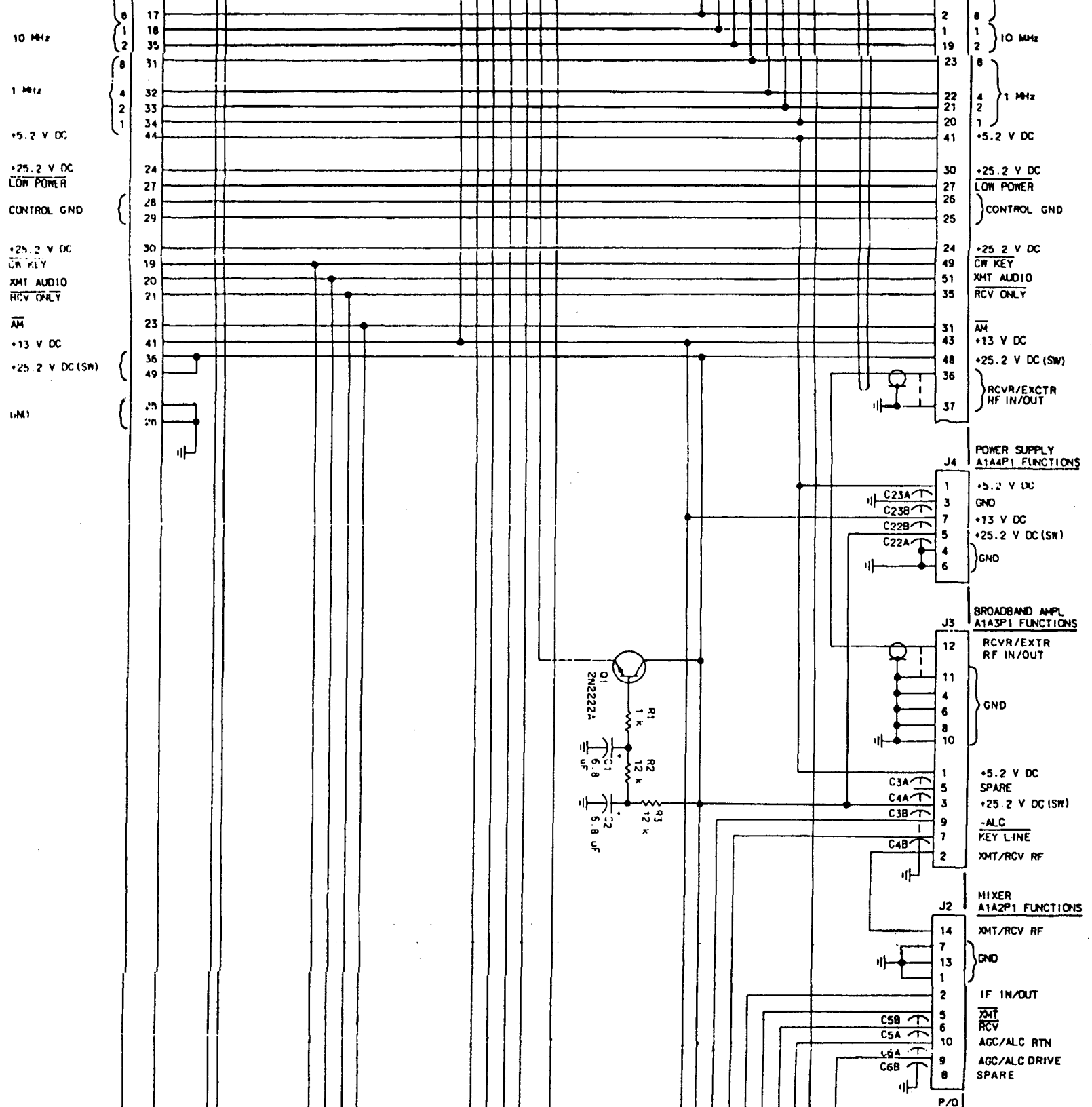
Figure 4-1. Chassis A1A1, Schematic Diagram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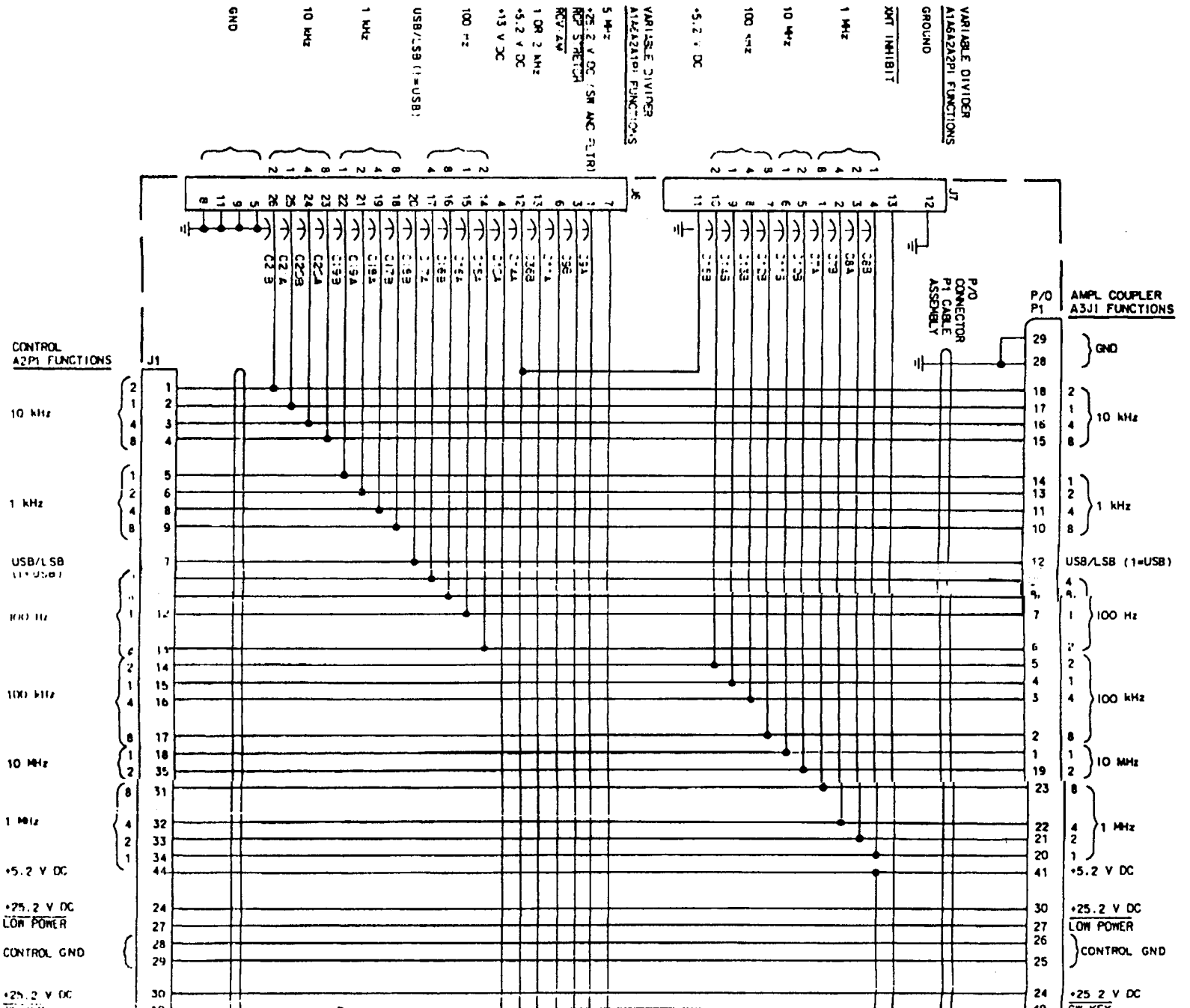
1 MHz
+5.2 V DC
+25.2 V DC
LOW POWER
CONTROL GND
+25.2 V DC
CW KEY
XMT AUDIO
RCV ONLY
AM
+13 V DC
+25.2 V DC (SW)
GND
17
18
35
31
32
33
34
44
24
27
28
29
30
19
20
21
23
41
36
49
10 MHz
1 MHz
+5.2 V DC
+25.2 V DC
LOW POWER
CONTROL GND
+25.2 V DC
CW KEY
XMT AUDIO
RCV ONLY
AM
+13 V DC
+25.2 V DC (SW)
RCVR/EXCTR
RF IN/OUT
POWER SUPPLY
A1A4P1 FUNCTIONS
J4
+5.2 V DC
GND
+13 V DC
+25.2 V DC (SW)
GND
C23A
C23B
C22B
C22A
BROADBAND AMPL
A1A3P1 FUNCTIONS
J3
RCVR/EXTR
RF IN/OUT
GND
+5.2 V DC
SPARE
+25.2 V DC (SW)
-ALC
KEY LINE
XMT/RCV RF
C3A
C4A
C3B
C4B
Q1
2N2222A
R1
1 k
R2
12 k
R3
12 k
C1
6.8 uF
C2
6.8 uF
MIXER
A1A2P1 FUNCTIONS
J2
XMT/RCV RF
GND
IF IN/OUT
XMT
RCV
AGC/ALC RTN
AGC/ALC DRIVE
SPARE
C5B
C5A
C6A
C6B
P/O


CONTROL
A2P1 FUNCTIONS
J1
10 kHz
1 kHz
USB/LSB
100 Hz
100 kHz
10 MHz
1 MHz
+5.2 V DC
+25.2 V DC
LOW POWER
CONTROL GND
+25.2 V DC
GND
10 MHz
1 kHz
USB/LSB (1=USB)
100 Hz
+13 V DC
+5.2 V DC
1 OR 2 kHz
5 MHz
VARIABLE DIVIDER
A1A6A2A1P1 FUNCTIONS
+5.2 V DC
100 kHz
10 MHz
1 MHz
XMT INHIBIT
GROUND
VARIABLE DIVIDER
A1A6A2A2P1 FUNCTIONS
J7
P/O
CONNECTOR
P1 CABLE
ASSEMBLY
P/O
P1
AMPL COUPLER
A3J1 FUNCTIONS
GND
10 kHz
1 kHz
USB/LSB (1=USB)
100 Hz
100 kHz
10 MHz
1 MHz
+5.2 V DC
+25.2 V DC
LOW POWER
CONTROL GND
+25.2 V DC